Technical Manual

DGC DISPLAY 6012

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DATA GENERAL TECHNICAL MANUAL

DGC DISPLAY

Model 6012

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SECTION I

INTRODUCTION

OBJECTIVE

This manual is intended for readers who need to understand the engineering prints for the DGC display 6012.

GENERAL

The DGC display is a cathode ray tube (CRT) I/O terminal used to enter, display, and edit alphanumeric data. It uses a non-interleaved, raster scan system for displaying data on the CRT screen. The display operates much like a teletype by transmitting a single character at a time but can also be used to enter and edit a full screen of data off line, and transmit it to the computer in a single burst. It will operate in full- or half-duplex mode, with odd or even parity, and with a choice of nine baud rates from 110 to 4800 baud. It is compatible with 20ma and 60ma current loop, and EIA type interfaces.

PHYSICAL DESCRIPTION

The display is a tabletop device, 13 inches high, 18 1/4 inches wide, and 23 1/4 inches deep. It consists of four major subassemblies; the display control board, the keyboard, the video monitor, and the power supply. These assemblies are mounted on a main chassis, and enclosed in a metal cover with a plexiglas cover over the video screen. Snap locks affix the cover to the main chassis. The following figure is an exploded view of the 6012 display.

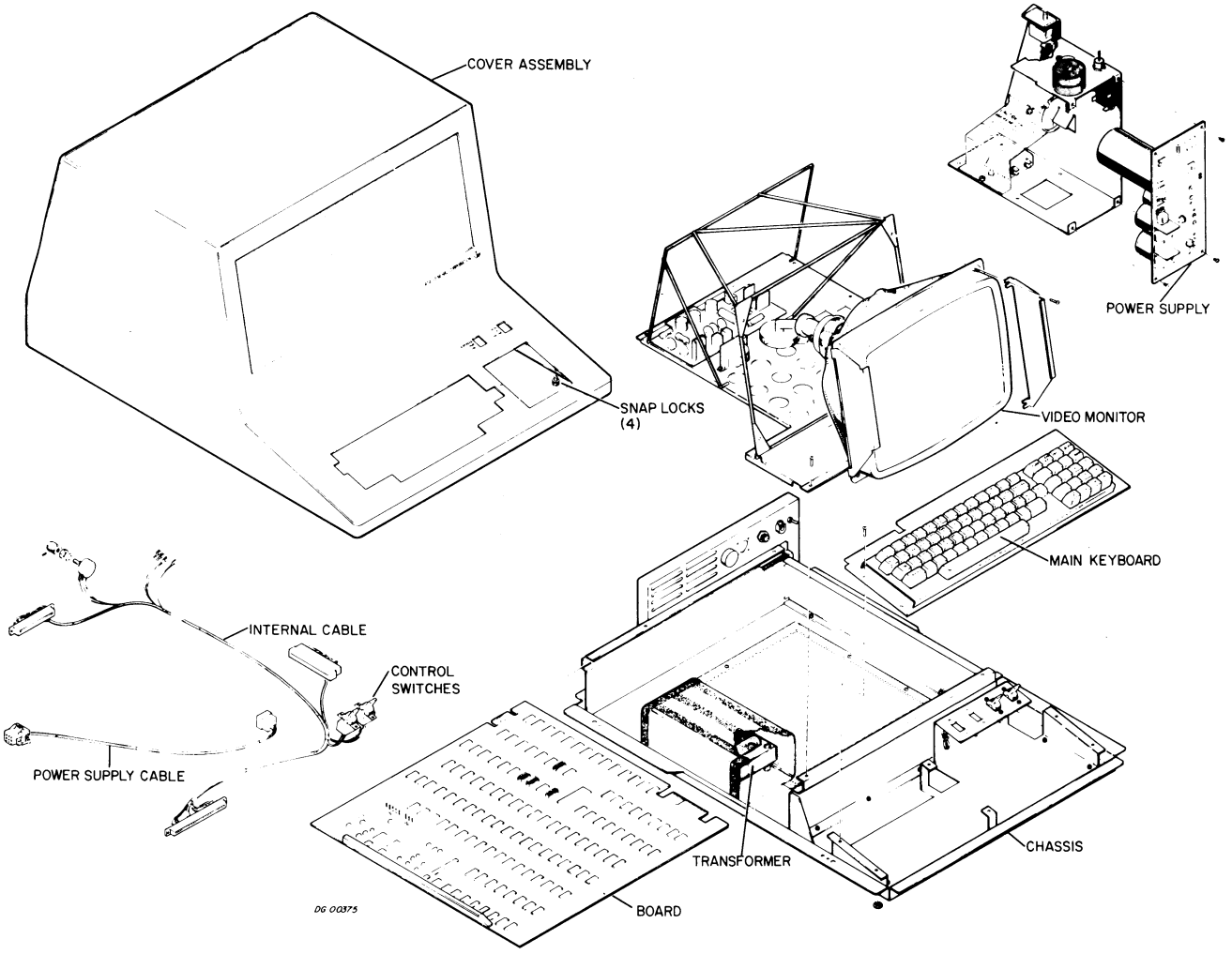
The display control board is a 15" by 15" printed circuit board, etched on both sides, with components mounted on the upper side. It includes both the receiver/transmitter section, and the display control logic. The board slides into a slot in the main chassis. The keyboard, monitor, and power supply are cabled to the display control board through removable connectors.

The keyboard is a mechanically switched, 73 station device which generates ASCII encoded data. It is mounted on the front portion of the chassis.

The video monitor is mounted on its own chassis, which is attached to the main chassis of the unit. Associated with it are a cathode ray tube for displaying data, and a printed circuit board which provides the power and drivers for the CRT beam. The display is a 9x12 inch screen with an active area of 6x9 inches.

The power supply assembly provides the power necessary for the display control board, the video monitor and the keyboard. It is mounted on the chassis, next to the video monitor.

6012 DISPLAY



LOGICAL OPERATION

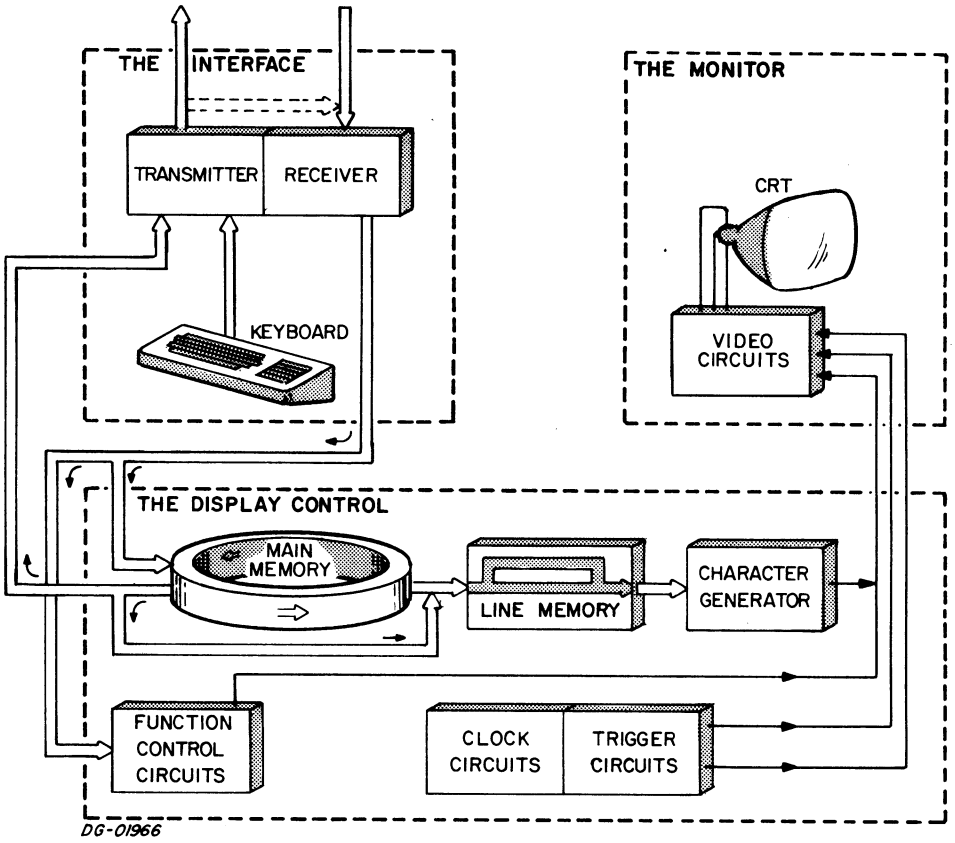
The purpose of an I/O terminal is to provide a communications link between the operator and processor. A link from the processor to the operator requires a display device with control logic to drive it, and an interface to the processor. For the link from the operator to the processor, a keyboard is used, with an interface and control logic to edit and verify data before transmission. To create this communication link, the DGC display is divided into three logical subsystems; the video monitor, the display control, and the interface.

The video monitor provides visual communication to the operator from the processor. The monitor consists of an electromagnetically deflected cathode ray tube display (CRT) and the video drivers necessary to operate it. A series of parallel, non-intersecting, horizontal lines called the raster is used to display the data on the CRT screen. Positions along these lines may be intensified at different places to create dots. The display control illuminates the dots in selected patterns that are recognized as alphanumeric characters on the screen. The CRT is refreshed continuously by data stored in the display control.

The display control stores and manipulates the data for refreshing the video screen. It consists of a main memory which stores the characters to fill the CRT screen, a line memory to store the character codes for the line being plotted, video drivers to generate the raster, control logic to control the functions the display may perform, and clock circuits to synchronize the system.

The interface controls the data flow between the operator, processor, and the display control. It consists of the receiver/transmitter, interface logic, and the keyboard. The receiver/transmitter controls data flow to and from the other subsystems. The interface logic is the direct link to the I/O controller in the processor. It provides the proper signals for the controller being used. The keyboard is the direct interface to the operator. It loads character codes into the transmitter to be sent to the processor or display control. The following diagram illustrates the data flow among the display subsystems.

6012 DISPLAY SIMPLIFIED BLOCK DIAGRAM



THIS MANUAL

This manual describes the logical operation of the DGC display 6012.

It is divided into six sections as follows:

SECTION I - explains the display's capabilities, and both physical and logical architecture.

SECTION II - explains the logical operation of the display's video monitor.

SECTION III - explains the logical operation of the display's control system.

SECTION IV - explains the logical operation of the display's interface system.

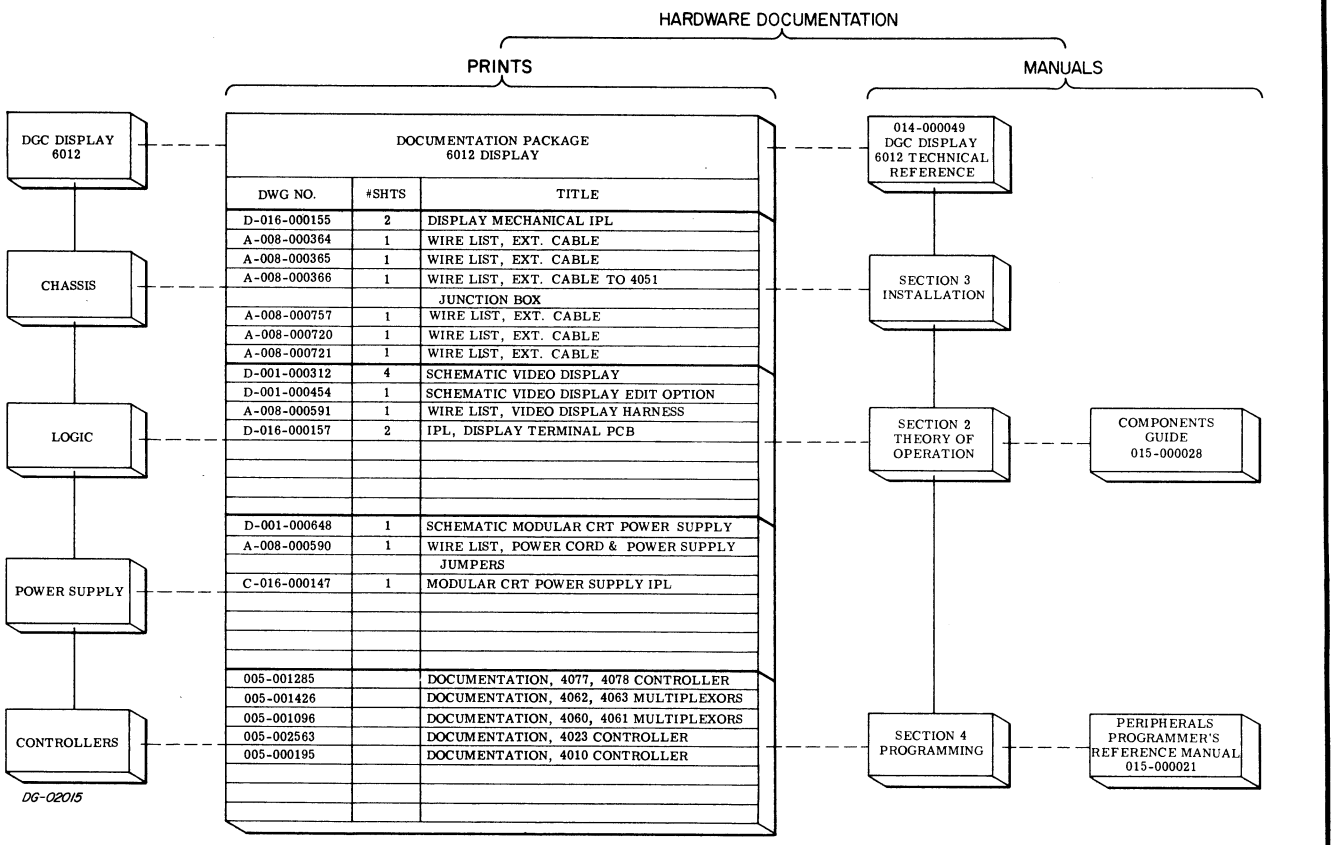
SECTION V - explains how the power supply works.

SECTION VI - describes maintenance and troubleshooting tips for the display.

RELATED DOCUMENTS

The following figure lists the engineering prints and manuals which describe the DGC display 6012. The "Peripheral Programmer's Reference Manual" (DGC #015-000021) describes, in detail, the programming of I/O devices, and the "Components Guide" (DGC #015-000028) gives logic diagrams and truth tables for the integrated circuits used in Data General equipment. It is assumed throughout this manual, that the reader has access to these documents.

6012 DOCUMENTATION



LOGIC CONVENTIONS

Drawings

Data General logic prints are drawn in close accordance with MIL-STD-806C. With this convention, logical functions are drawn as physically implemented. That is, where discrete gates are used to implement a function, these gates are shown. On the other hand, where a more complex integrated circuit is used, for instance a multiplexor, the function it performs is shown as a rectangular box.

Signal Levels

Throughout this manual, a distinction is frequently made between electrical levels and logical values. To minimize confusion, electrical levels are always indicated by an "H" or "L", and logical values by a "1" or "0". As an electrical level, and "H" indicates that the signal is high (greater than +1.7 volts) and an "L" indicates that it is low (less than +0.7 volts). An asserted, or true signal is indicated by a logical "1" and a false signal by a "0".

Signal Names

In Data General equipment the assertion state of a signal can be either low or high, depending upon how it is defined. To distinguish between the two types of signals a naming convention has been adopted which defines the relationship between the logical value and the electrical level of a signal. If the signal includes a horizontal bar over the name, as "$\overline{\text{WRITE}}$", then that signal is asserted when it is at a low electrical level. Conversely, a signal without the bar "WRITE", is asserted when high.

Closely related, or bussed, signals are indicated effectively by subscripting a common label. For instance, suppose that BUS 0 through BUS 5 are all required to completely specify a function. All or part of such a group of signals is identified by placing brackets around the range of subscripts included, as BUS<0-5>. In this case, the suffix carries the information that there are six BUS lines under discussion, from BUS 0 through BUS 5, inclusive.

Two signals having the same name but differing by the bar almost always refer to the same logical function and are electrical inverses of each other. Thus $\overline{\text{WRITE}}$ will be low when WRITE is high, and the two signals will be true at the same time.

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SECTION II

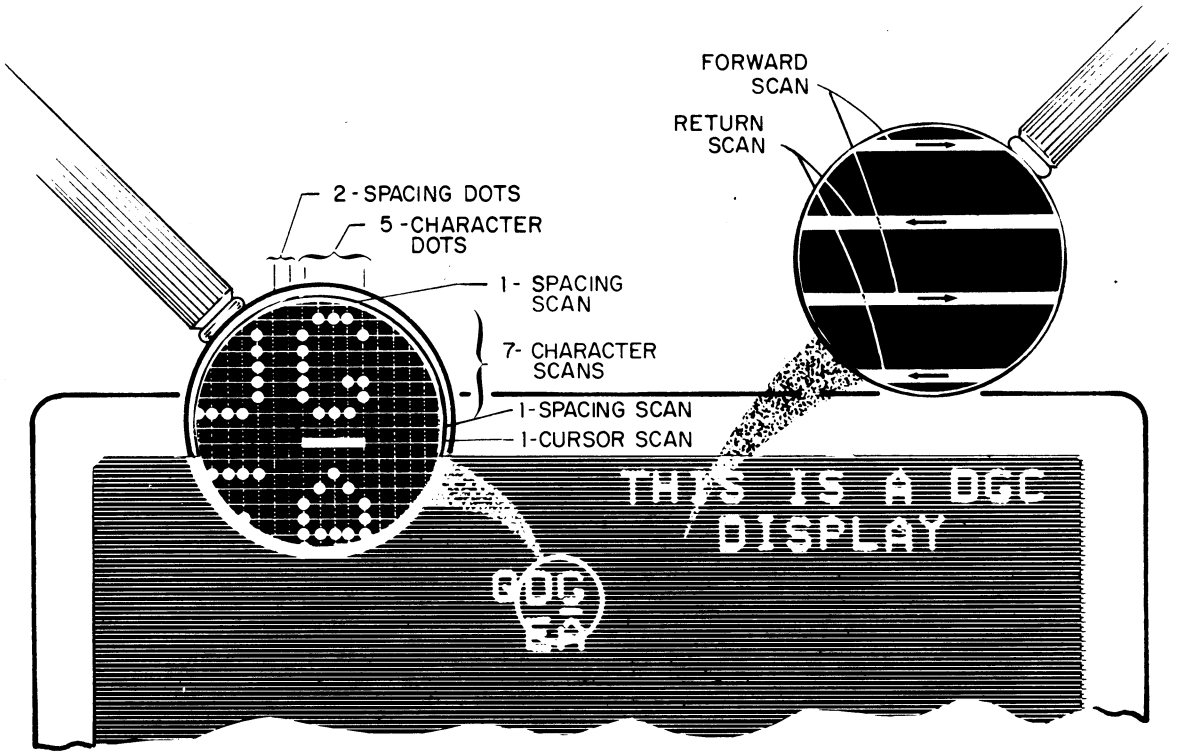
THE VIDEO MONITOR

THE VIDEO MONITOR

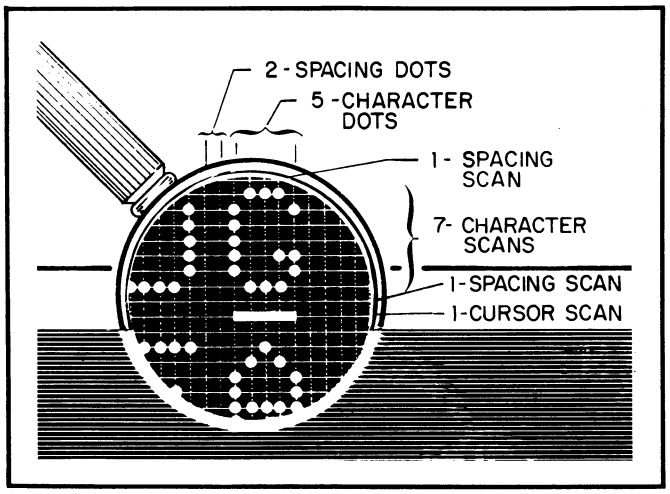
The video monitor is the display's output to the operator. It uses a pattern of lines traced with an electron beam to display character codes stored in the display's memory as alphanumeric characters on a twelve inch, cathode ray tube (CRT). The monitor is a magnetically deflected device which uses a non-interleaved raster pattern of scanning as shown below. It is triggered and synchronized by the display control logic and consists of electromagnetic deflection circuits to move the CRT's electron beam horizontally and vertically around the screen plus a video generator to control its intensity. The electron beam scans the screen to display 24 lines of alphanumeric data, 80 characters wide.

The monitor uses a system of parallel horizontal lines to display characters on the CRT screen. This system is known as the raster. Discrete positions within the raster are defined in the display control logic by a number of parameters; line, scan, character, and dot positions. There are 24

SCANNING PATTERN



lines displayed in the screen's active area (it has additional spacing for margins at top, bottom and sides), each line consisting of 10 horizontal scans. As the monitor's electron beam makes each horizontal scan, it traces one slice of a line. These scans are divided into 80 character positions across the screen. Each character position is divided into 7 dot positions in which the electron beam may be intensified (unblanked), or held at a low enough intensity so as not to leave a visible trace on the screen (blanked). This scanning produces a character field made up of 7x10 distinct dots. The actual synchronization and control of the raster is external to the monitor, contained in the display control logic.



The monitor's deflection circuits are synchronized and triggered to produce the trace as shown above by separate signals derived in the display control logic. The horizontal deflection circuit is synchronized to a 15.6KHz signal from the display control, and creates a sawtooth current which drives the electron beam across the CRT face. It will run at nearly this frequency if the sync pulse is absent, but synchronization is necessary to ensure the proper alignment between scans. The vertical deflection circuit is triggered by a 60Hz signal from the display control and creates a current sawtooth which drives the electron beam down the screen. The vertical drive will not run without the 60Hz trigger pulse. This combination of scanning frequencies produces 240 horizontal scans for each vertical scan.

A detailed description of the monitor, including troubleshooting guides may be found in the vendor supplied instruction manual.

Caution When working around or troubleshooting the monitor, be aware that:

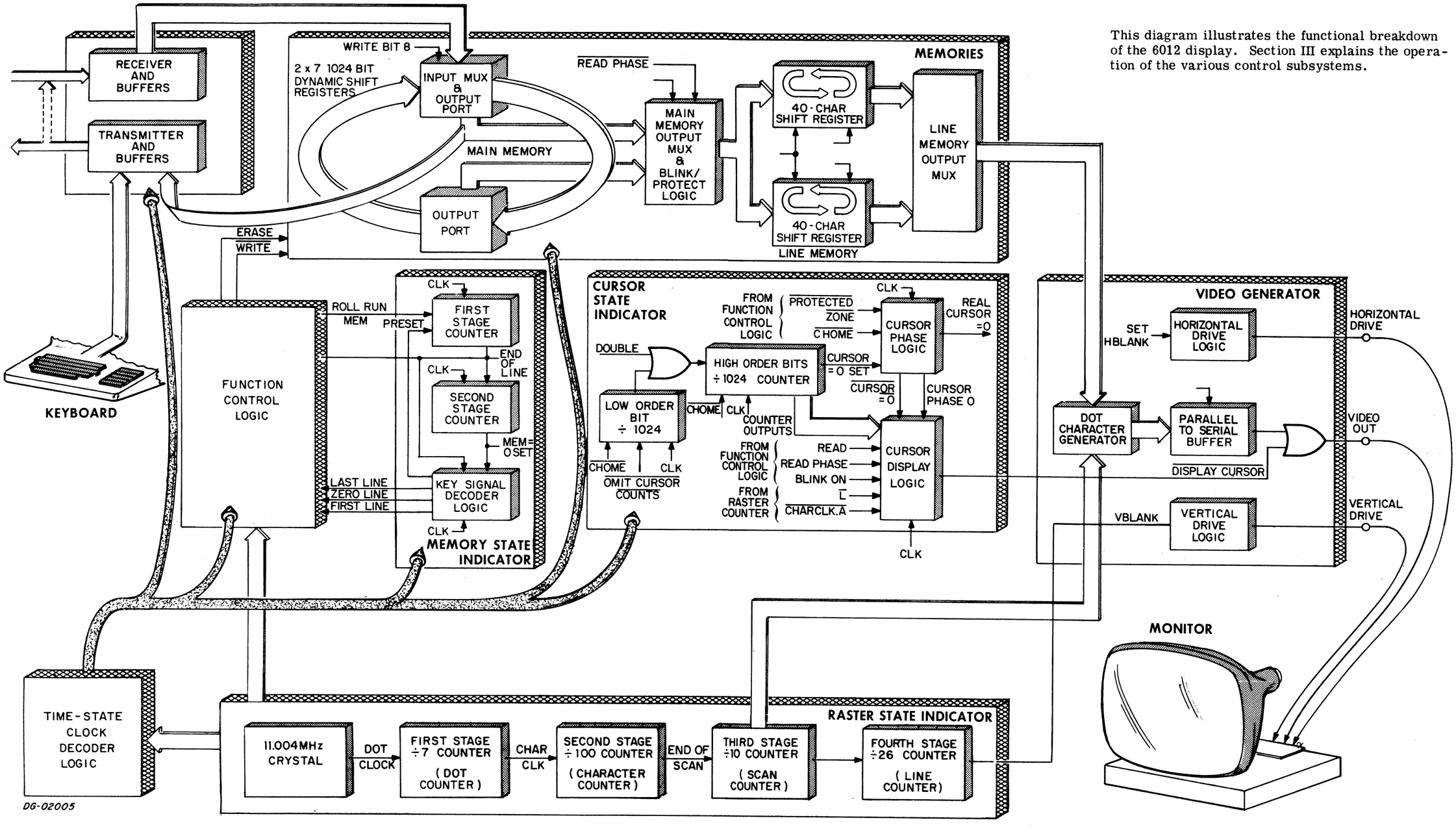
1. There is a high voltage power supply in the monitor which can cause a severe shock.
2. The cathode ray tube may implode if cracked.
3. The monitor has been adjusted at the factory and no further adjustment should be necessary.
4. Only technicians familiar with the operation of television monitors should attempt to repair the display monitor.

REFERENCES

1. Prints - The Display Receiver/Memory 001-000312-09.

6012 DISPLAY FUNCTIONAL BLOCK DIAGRAM

This diagram illustrates the functional breakdown of the 6012 display. Section III explains the operation of the various control subsystems.



SECTION III

THE DISPLAY CONTROL

INTRODUCTION

The display control receives data from the interface, interprets command codes, stores character codes in a memory, and returns data to the interface when necessary. It controls the raster, triggers the monitor, and continuously refreshes the CRT screen with the proper signals for the characters stored in memory.

The display control maintains various registers, memories, and controls that correlate and sometimes alter the sequence of logical events which take place in the display. They are a raster state indicator to synchronize the display logic and monitor, recirculating memories for storage, a memory state indicator to follow data as it circulates in the memories, a cursor position indicator to follow the position where data will be stored in main memory, video control logic to create the necessary video signal, and the command code controller to interpret and perform various commands from the keyboard or processor.

THE RASTER STATE INDICATOR

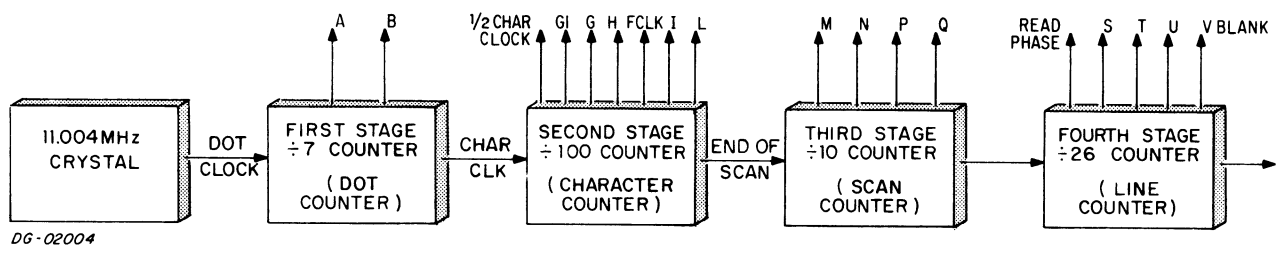
The raster state indicator is a series of counters which synchronize the display control and video monitor. It consists of a dot counter, a character counter, a scan counter, and a line counter each of which clocks the next higher stage. These counters determine the proper timing for each dot, character, scan, and line position on the CRT screen, and provide signals to trigger both horizontal and vertical sync pulses.

The counters are driven by a crystal oscillator, the period of which defines the basic screen interval known as the dot. This oscillator operates at 11.004MHz, cycling 182,000 times during an entire scan of the screen.

As the signals which determine dot positions are generated, they are counted by the first stage counter called the dot counter. This divide by seven counter provides timing signals for the seven dot positions in each character field. It determines horizontal blanking for spaces between characters and timing for the video control logic.

Every cycle of the dot counter is one character field across the CRT face. These character fields are defined by the second stage counter called the character counter. This counter provides timing for the 80 character fields on the video screen. It also provides the timing for the equivalent of an additional 20 character fields for the horizontal retrace of the electron beam. Each cycle of this counter is one scan.

RASTER STATE INDICATOR BLOCK DIAGRAM



The ten scans which make up each line are counted by the divide by ten scan counter. This counter provides scan numbers to the video generator for proper dot generation and signals to the main and line memory clock generators for proper synchronization between the memories. During each cycle of the scan counter, one full line of data is displayed on the screen.

The final stage of the raster timer is the divide by 26 line counter. This counter increments on each cycle of the line counter and tracks each of the 24 lines of displayed data as well as the equivalent of 2 line cycles for vertical retrace of the electron beam. Upon final count of 26 lines, the counter waits for a 60Hz sync pulse, and begins the entire screen refresh cycle again.

THE DISPLAY MEMORIES AND THEIR STATE INDICATORS

There are two distinct memories used in the display control system, the main memory, and the line memory. Both memories are made up of shift registers and recirculate almost continuously. The main memory stores the 1920 characters necessary for refreshing the video screen. The line memory stores all the characters in the line presently being plotted on the CRT screen. It is refreshed from main memory on every tenth cycle. Associated with the memories are a memory state indicator and a cursor state indicator. The memory state indicator is used for tracking key screen positions as they circulate in main memory, and a cursor state indicator points to the position where new data will be entered into the memory.

The Display Memories

The display main memory is a 2048 character recirculating semiconductor memory, in which the 1920 characters displayed on the CRT screen are stored as the 64 ASCII alphanumerics and those control codes which delimit protect and blink fields. The memory consists of two 7x1024 bit MOS dynamic shift registers and is divided into 25 sections called lines, numbered 0 through 24. Line 0 always contains 128 blank (octal 40) character codes. Eighty of these line zero characters are used when in Roll Mode to fill the bottom line of the screen with blanks. All other lines are used to store data and are 80 characters in length. Only 6 bits are necessary to define the 64 character set, the seventh bit in the recirculating memory is used to differentiate between a character and the blink or protect control codes stored in memory.

Main memory is loaded through a single port directly from the output of the interface. Signals from the command code controller determine the proper insertion of data into main memory. The command code controller allows only characters and blink or protect control codes to be stored in the memory. The 64 ASCII alphanumerics contain only the codes for upper case letters; lower case codes are translated into upper case by changing their high order bit prior to loading the character into memory.

The main memory is accessed for reading from two ports located 1024 characters apart. Two ports are necessary because the main memory shifts only halfway around during a line cycle. The line memory needs to be loaded with a new line of data at the end of each line cycle. By shifting halfway around for each line cycle, the MOS memory will be shifting at a slower rate, well within its operating specifications.

An 80 character line memory provides data to the video control logic. It consists of two 6x40 bit shift registers. One shift register stores the even numbered characters and the other stores the odd numbered characters in the line to be displayed. Multiplexors at the output of the shift registers control the proper ordering of the characters being presented to the video control logic. Each line is displayed as 10 scans of the electron beam (numbered 0 through 9); the line memory is refreshed from one of two main memory ports on the tenth scan. Loading is accomplished by inserting characters for the next line into their proper sections of line memory until the entire line has been refreshed. Blink and Protect control codes are converted to blanks prior to loading.

The Memory and Indicator Clocks

The dynamic design of main memory requires it to shift almost continuously in order to retain stored data. To satisfy this requirement, the main memory loads the line memory from one port during the tenth scan of a line, and then shifts such that the next line of characters is at the other main memory port when the line memory has completed nine scans of the next line. The next line is loaded into main memory from this port. For a review of dynamic shift registers, their operation and application requirements, see Appendix C.

During a typical line cycle, the main memory clocks operate in three modes; Slow, Fast, and Stop. Slow mode is used primarily for loading of the line memory during the tenth scan; it shifts main memory at the same rate as line memory. Fast mode is a transit mode during which the main memory is shifted to the next main memory port,

1024 locations away, at a rate 7/5 the speed of the line memory. A certain overlapping exists between these modes, for Slow mode extends into the transit time between ports. The clocks can be stopped for a short period of time, in order to synchronize the main and line memories; this is Stop mode. With only Fast mode and Slow mode clocks, main memory would be ready to load the line memory long before the line memory had completed nine scans; Stop mode inserts short pauses in the main memory clocks to synchronize the main and line memories.

There are three distinct sequences of Fast, Slow, and Stop mode clock pulses; normal, vertical retrace, and roll run. These sequences are necessary to control the relationship between the main and line memories for special lines and commands. The normal line sequence occurs while tracing any of the displayed lines of data. The vertical retrace cycle occurs at the end of a screen refresh for the equivalent of two lines of data (20 circulations of line memory). It shifts the zero line past the main memory ports, synchronizing the main memory for loading of the first line of data into the line memory. During this time, the electron beam returns to the top of the screen. The roll run sequence is used to roll the screen up one line in Roll mode. It occurs while the first line is being displayed on the screen. The following table lists the various line cycles, their characteristics, and their relationship to the line memory clocks.

MAIN MEMORY CLOCK CYCLES

Clock Modes	Main Memory Shifts	Line Memory Shifts
	NORMAL LINE CYCLE	
FAST SLOW STOP	700 404 --- 1104 80 to Load Line Memory +1024 to shift to next Main Memory port	500 404 96 1000 10 times around Line Memory = 1 Line
	VERTICAL RETRACE CYCLE	
FAST SLOW STOP	700 388 --- 1088 for two lines 128 shifts to pass zero line +2048 for one full recirculate	500 388 112 1000 for two lines 20 times around line memory = 2 lines
	ROLL RUN LINE CYCLE	
FAST SLOW STOP	700 484 --- 1184 80 shifts to skip line +80 shifts to load line memory +1024 to shift to next Main Memory port	500 484 --- 1000 10 times around line memory = 1 line

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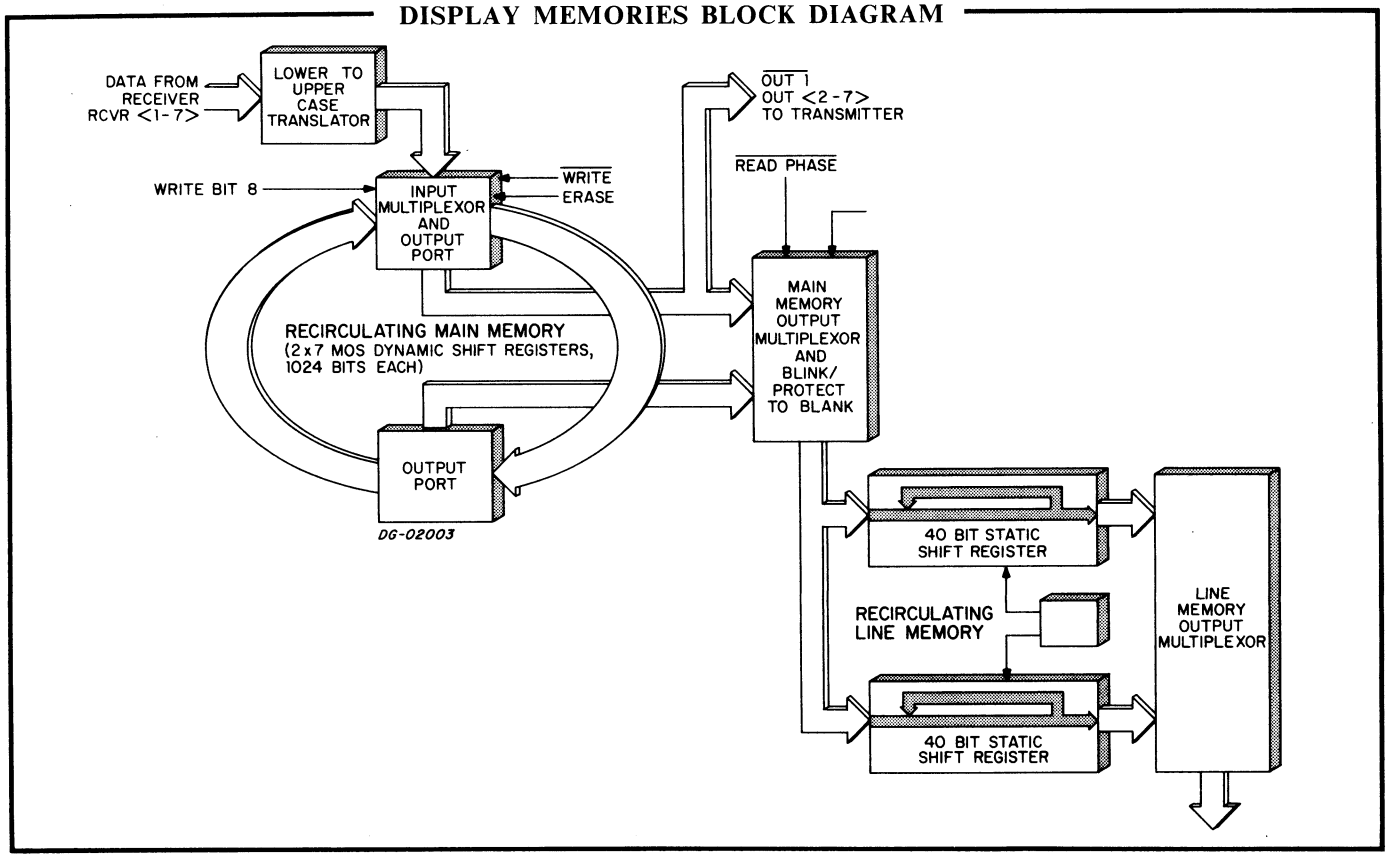
III

DISPLAY MEMORIES BLOCK DIAGRAM



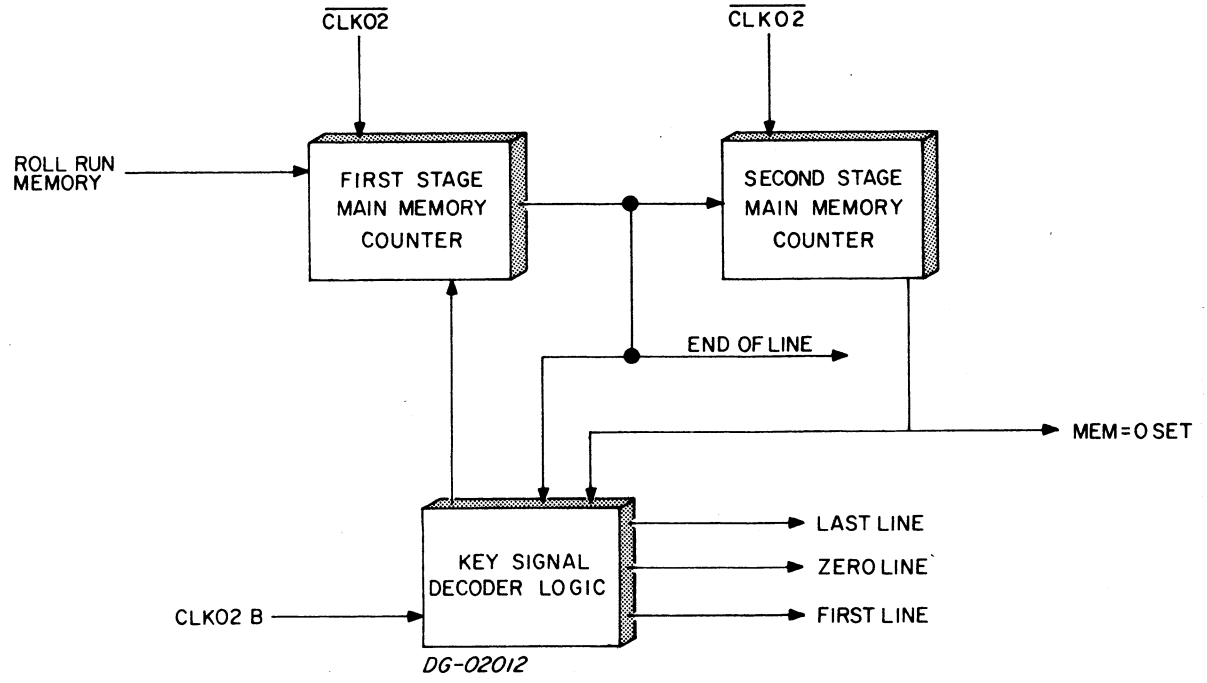
The Memory State Indicator

The memory state indicator preserves the relationship of every line stored in memory to its correct position on the CRT screen. It defines the last character position in each line, and the first, last, and zero (unused) lines as they pass the main memory output multiplexor. Tracking these lines is important since many of the commands to insert characters and move the cursor depend upon the position of the first, last, and zero lines in main memory. The state indicator is clocked by the same clocks as main memory and is divided into two distinct stages. The first stage tracks the characters in each line, and the second stage tracks the lines themselves.

The first stage denotes the end of each line. This is done by counting the 80 shifts as each of the 24 displayed lines passes the main memory output multiplexor and 128 shifts of main memory for the zero line. Each time the counter overflows, it indicates the end of a line passing the main memory output multiplexor.

The second stage is a counter which tracks the 24 active lines stored in main memory. It denotes the first, last, and zero lines in main memory. On overflow of the second stage, a signal denotes that the last line is passing the main memory output multiplexor. On the next end of line signal, a signal denoting zero line asserts during the time it is passing the main memory output multiplexor. Finally, as the first line passes the main memory output multiplexor, a signal denoting first line is asserted, and the second stage again tracks the 24 active lines as they circulate in main memory.

MEMORY STATE INDICATOR BLOCK DIAGRAM



The Cursor Position Indicator

As main memory circulates, the cursor position indicator tracks the position where new data will be entered. It denotes the time when the cursor position is passing the main memory input multiplexor and generates a signal for the video control logic to display a blinking underscore on the video screen at the point where new characters may be entered. The cursor state indicator is divided into three sections; a cursor phase pointer, a 10 bit binary counter, and cursor display logic.

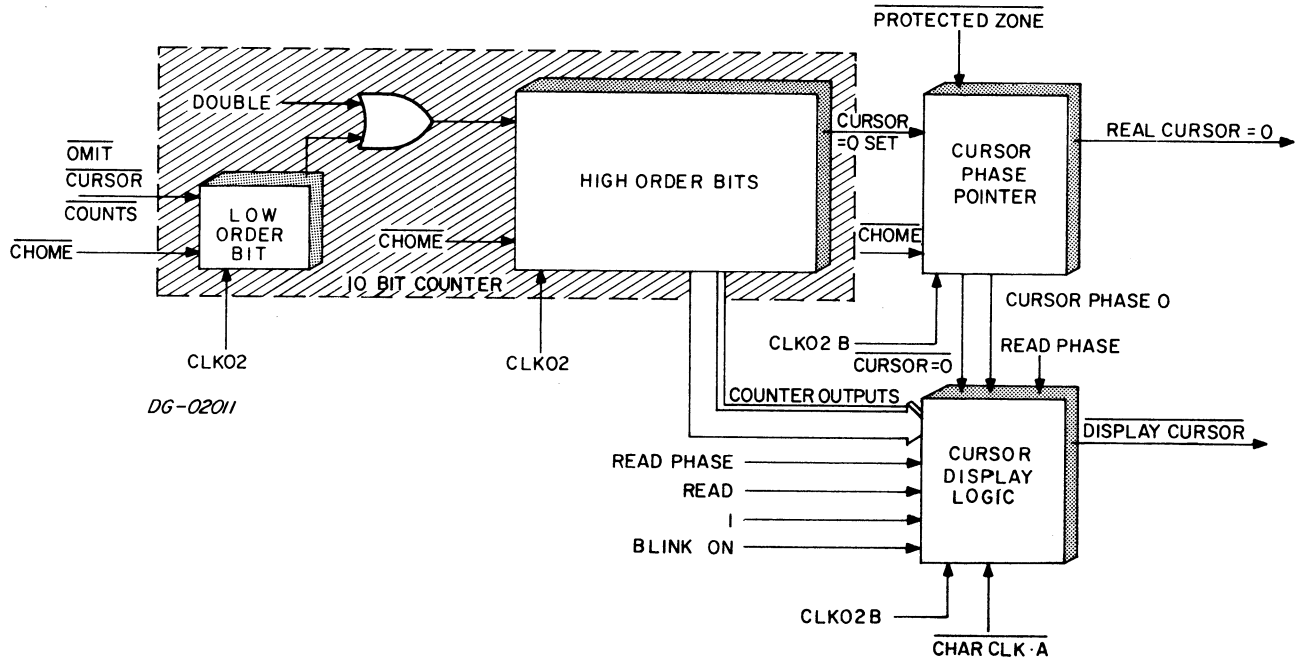
The two state cursor phase pointer is a register indicating which half of main memory contains the character at the current cursor position. It changes state as that character position passes a main memory port.

The 10 bit binary counter tracks the cursor as it moves within either half of main memory. When the character at the cursor position passes a main memory port, this counter resets to zero and then begins to track the cursor position through the second half of main memory. Each time this counter resets to a value of zero, the cursor phase pointer changes state.

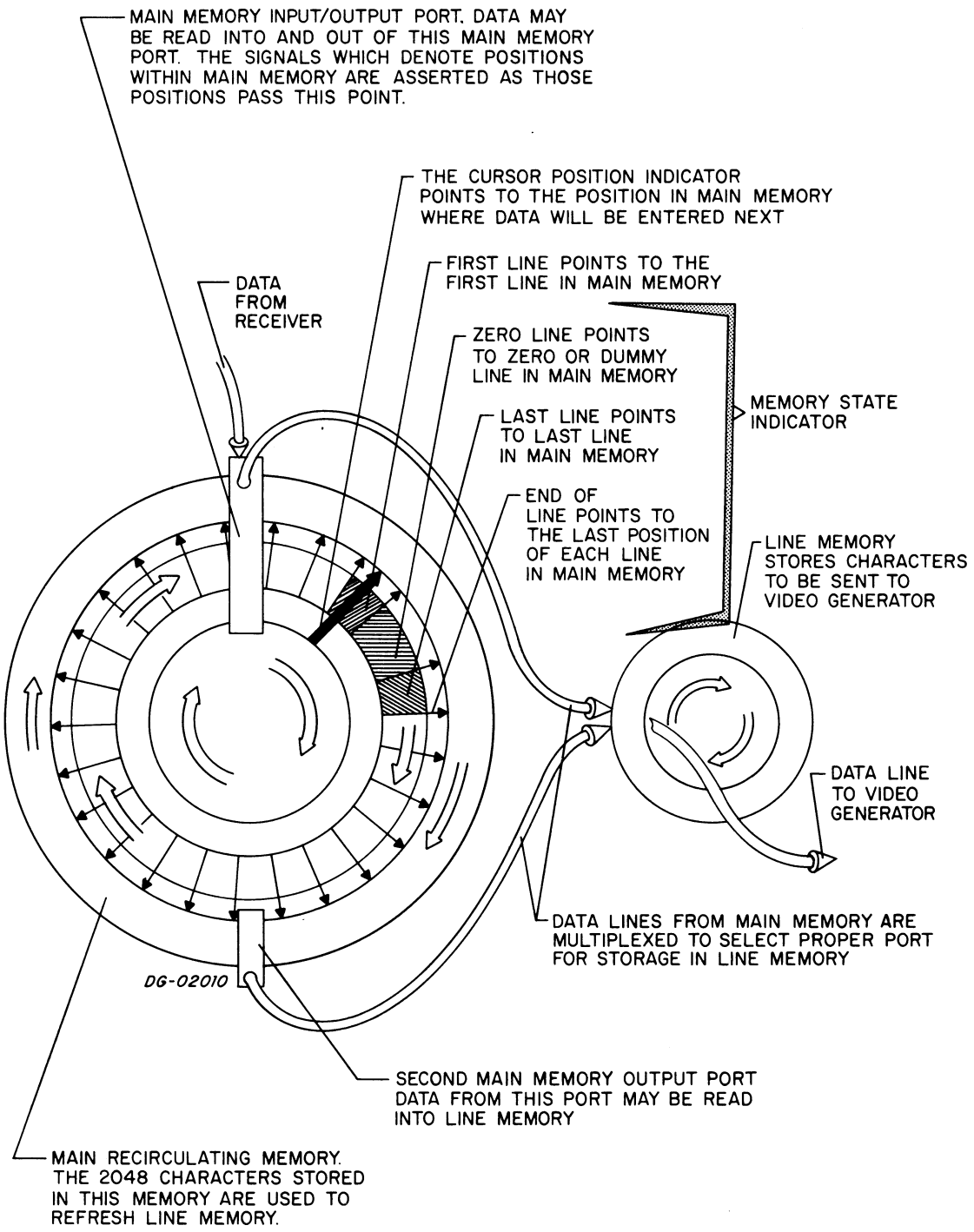
The cursor display logic generates the video signal that displays the cursor position on the CRT screen. The video signal is derived during the tenth scan of a line, and is dependent upon the state of the cursor phase pointer and the 10 bit binary counter. A delay exists between the time the cursor state indicator is indicating the cursor position and the cursor display logic actually sends the video signal. This delay is the same as the delay between the time the character in the cursor position is loaded into line memory and the time it is displayed on the screen. The delay in the cursor display logic causes the cursor position to be displayed under the proper character.

During a normal cycle, the cursor position indicator is clocked along with main memory. When any command which moves the cursor position is given, the cursor position indicator must be clocked faster or slower, to change its relation to main memory, causing it to overflow earlier or later. For example: the cursor moves one position to the right when a clock pulse to the 10 bit counter is skipped, forcing it to overflow one character later; similiarly, the cursor moves one position to the left when the first bit of the counter is stopped and the second bit of the counter is clocked with main memory instead, forcing the counter to overflow one character earlier. All cursor movement is implemented by varying numbers of the above commands, up being the equivalent of 80 cursor left commands, down being 80 cursor right commands. Home is implemented by resetting the counter until the first character of the first line passes a main memory port.

CURSOR STATE INDICATOR BLOCK DIAGRAM



MEMORY TIMING



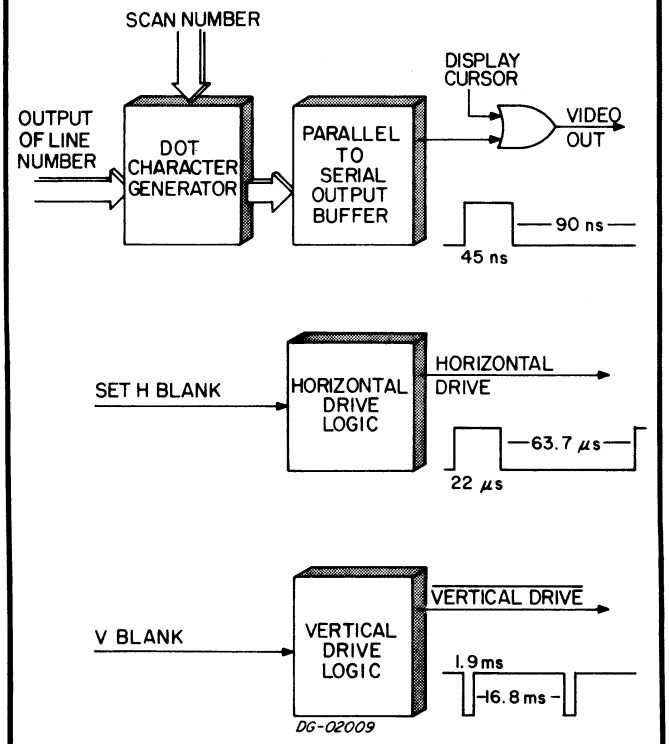
The main memory, line memory, memory state indicator, and cursor state indicator can be visualized as a number of synchronized, rotating wheels. The line memory is rotating at a constant speed and provides data for the video generator. The main memory rotates in such a manner that for every ten circulations of the line memory, it rotates half way around plus one line. It speeds up and slows down so that on every tenth circulation of the line memory, both are circulating at the same rate. It is during its tenth circulation that line memory is loaded with the next line of data from main memory as the data passes an output port.

The memory state indicator and the cursor state indicator normally circulate at the same rate as the line memory. The signals generated by both indicators (denoted by arrows) determine the ends of lines, cursor position, last, zero and first lines in main memory. The relation of these positions to the actual data stored in main memory can be changed by slowing or speeding the indicators with relation to the main memory. Since the main memory can be loaded with data only from the main memory input port, these key positions are simply flagged when they pass the port.

THE VIDEO CONTROL LOGIC

The video control logic determines the vertical and horizontal trigger and blanking signals to the monitor. It consists of vertical and horizontal trigger logic and a character dot generator to determine the proper video signal.

VIDEO CONTROL LOGIC BLOCK DIAGRAM



The vertical and horizontal trigger circuits are driven by signals derived from the raster state indicator. They are synchronized to trigger horizontal scans of the CRT beam at 15. 6KHz, and to trigger the vertical deflection of the CRT beam at 60Hz.

The video signal to the monitor is derived in a read-only-memory called the dot character generator. The ASCII code and scan number for the character to be plotted are fed to the character generator. The ROM then determines the proper video signal for the character and scan to be plotted. The signals generated are in parallel form and are shifted through an output buffer which converts them to serial form with the proper spacing between characters. If the cursor is in this line, it is displayed on the tenth scan by a video signal derived by the cursor position indicator.

THE COMMAND CODE CONTROLLER

The display command code controller is used extensively throughout the display to control the entering of data, the mode of operation, and to perform editing functions. Characters are received, decoded, and the specified functions are then performed. The function control logic writes the 64 ASCII characters into memory, and allows seven cursor movement functions; LEFT, RIGHT, UP, DOWN, CARRIAGE RETURN, TAB, and HOME. The logic also performs TRANSMIT BUFFER, ERASE TO END OF LINE, CLEAR, and FORCE ERASE commands. Protect and blink logic allows portions of the screen to be protected or to blink.

III

REFERENCES

1. Prints- The Display Receiver/Memory 001-000312-09
2. Prints- Video Display Edit Option 001-000454-07

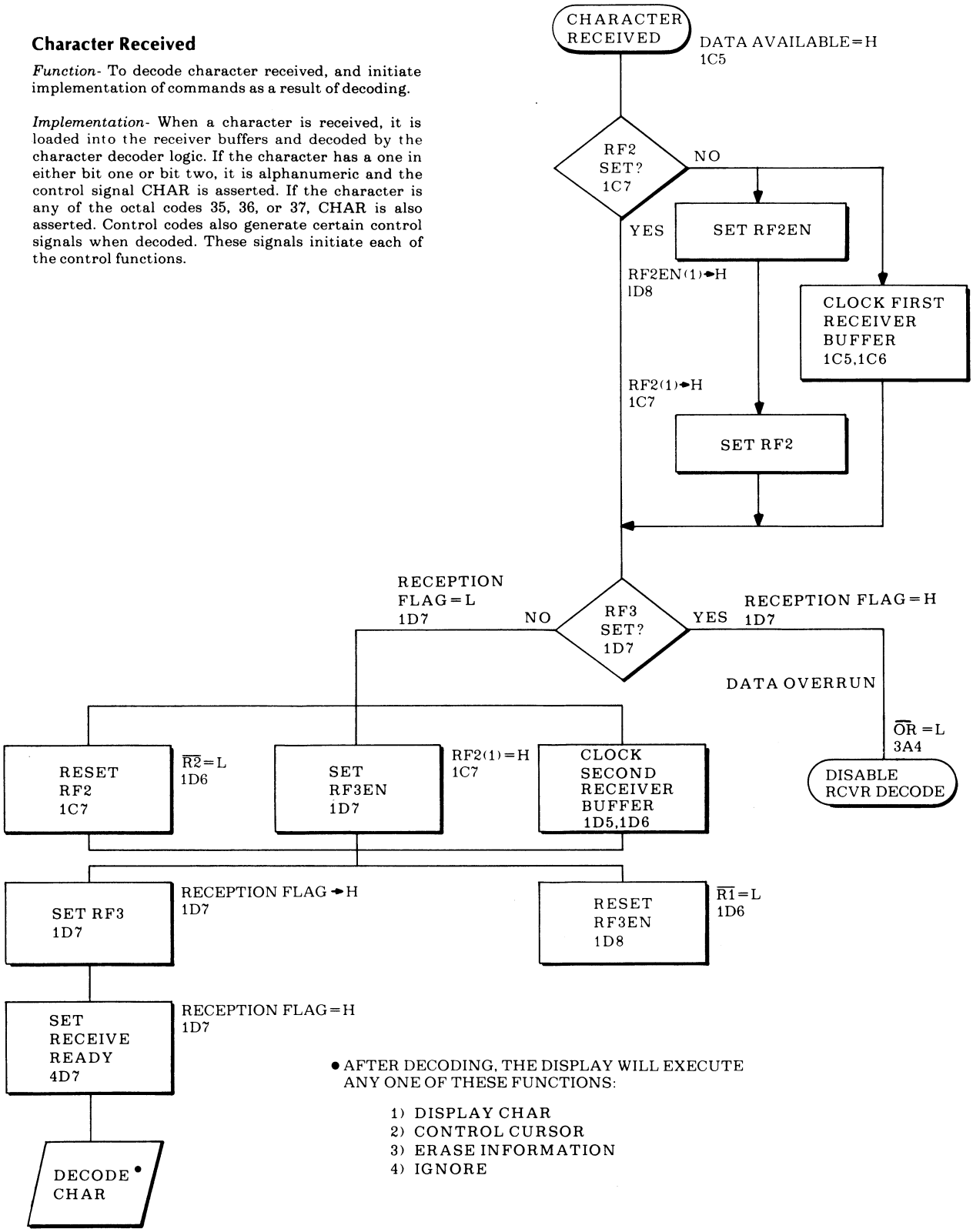
FLOW DIAGRAMS

The following flow diagrams show the various functions of the 6012 display.

Character Received

Function- To decode character received, and initiate implementation of commands as a result of decoding.

Implementation- When a character is received, it is loaded into the receiver buffers and decoded by the character decoder logic. If the character has a one in either bit one or bit two, it is alphanumeric and the control signal CHAR is asserted. If the character is any of the octal codes 35, 36, or 37, CHAR is also asserted. Control codes also generate certain control signals when decoded. These signals initiate each of the control functions.



- AFTER DECODING, THE DISPLAY WILL EXECUTE ANY ONE OF THESE FUNCTIONS:

  1) DISPLAY CHAR
  2) CONTROL CURSOR
  3) ERASE INFORMATION
  4) IGNORE

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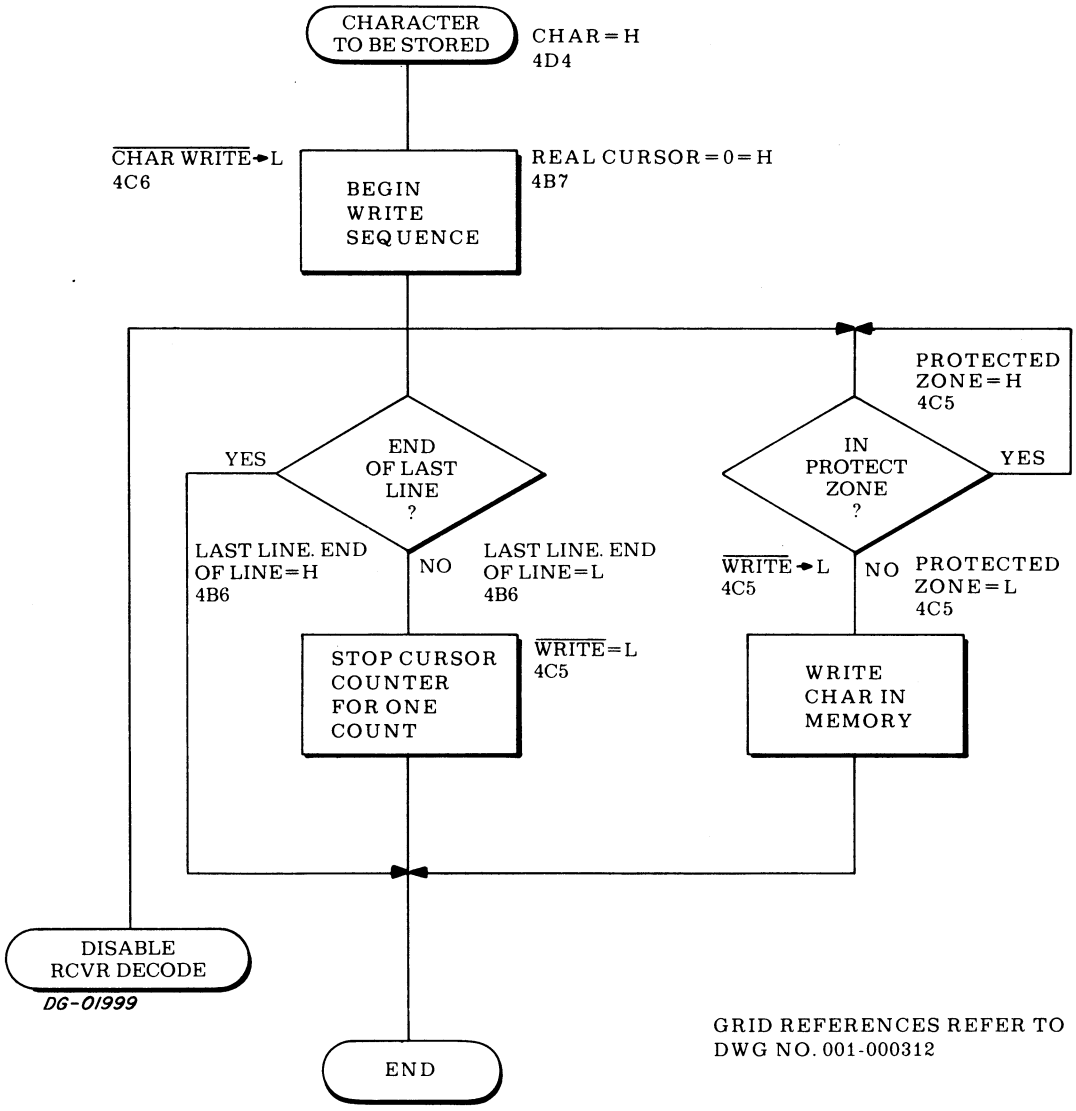
GRID REFERENCES REFER TO DWG NO. 001-000312
END

Stored Character

Function- Stores any of the 64 ASCII character codes and blink/protect control codes in the display's main recirculating memory.

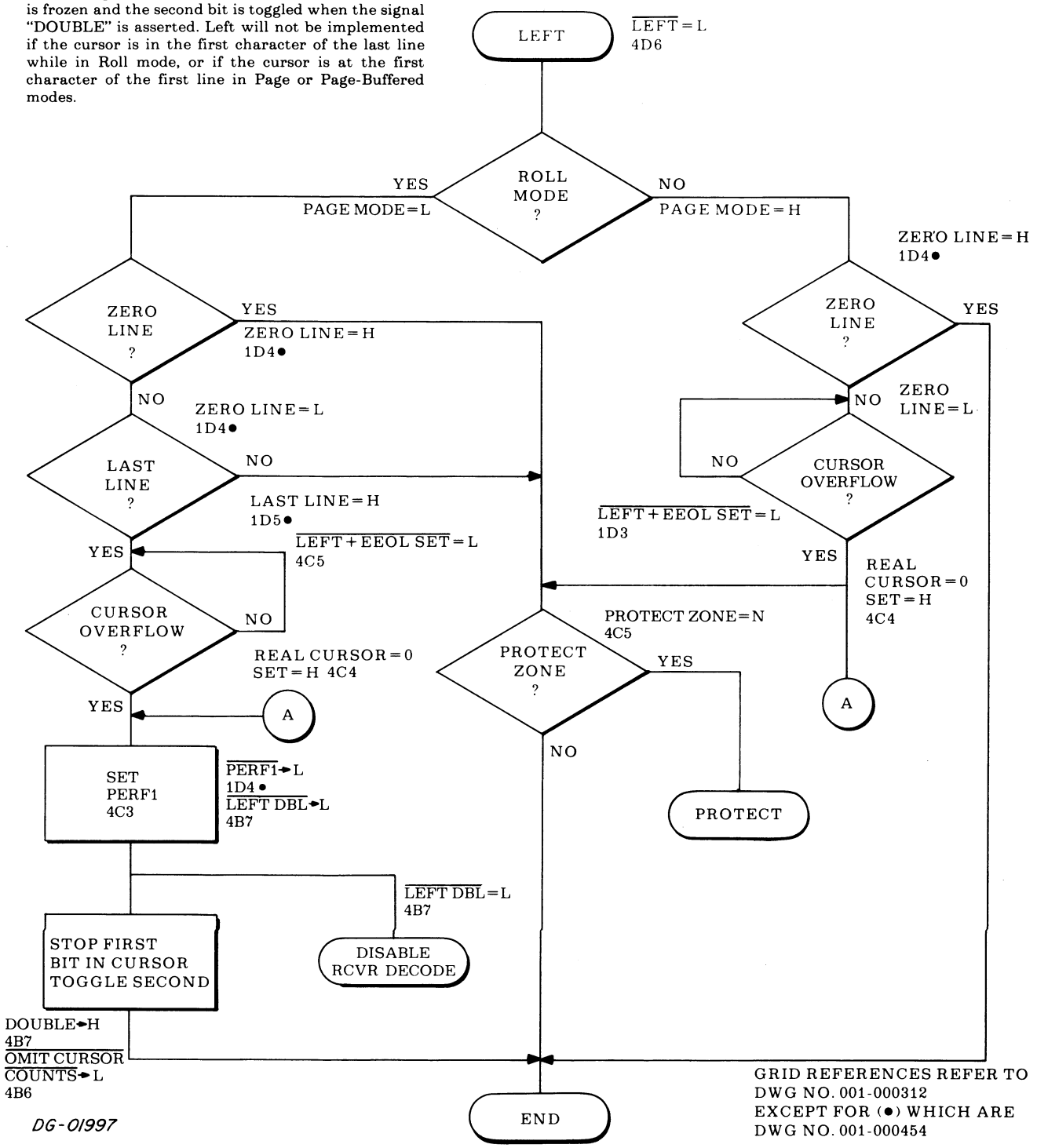
Implementation- When the cursor position passes the main memory input multiplexor, the received character is stored in main memory and the cursor is moved one position to the right.



Left

Function- Moves the cursor left one character position.

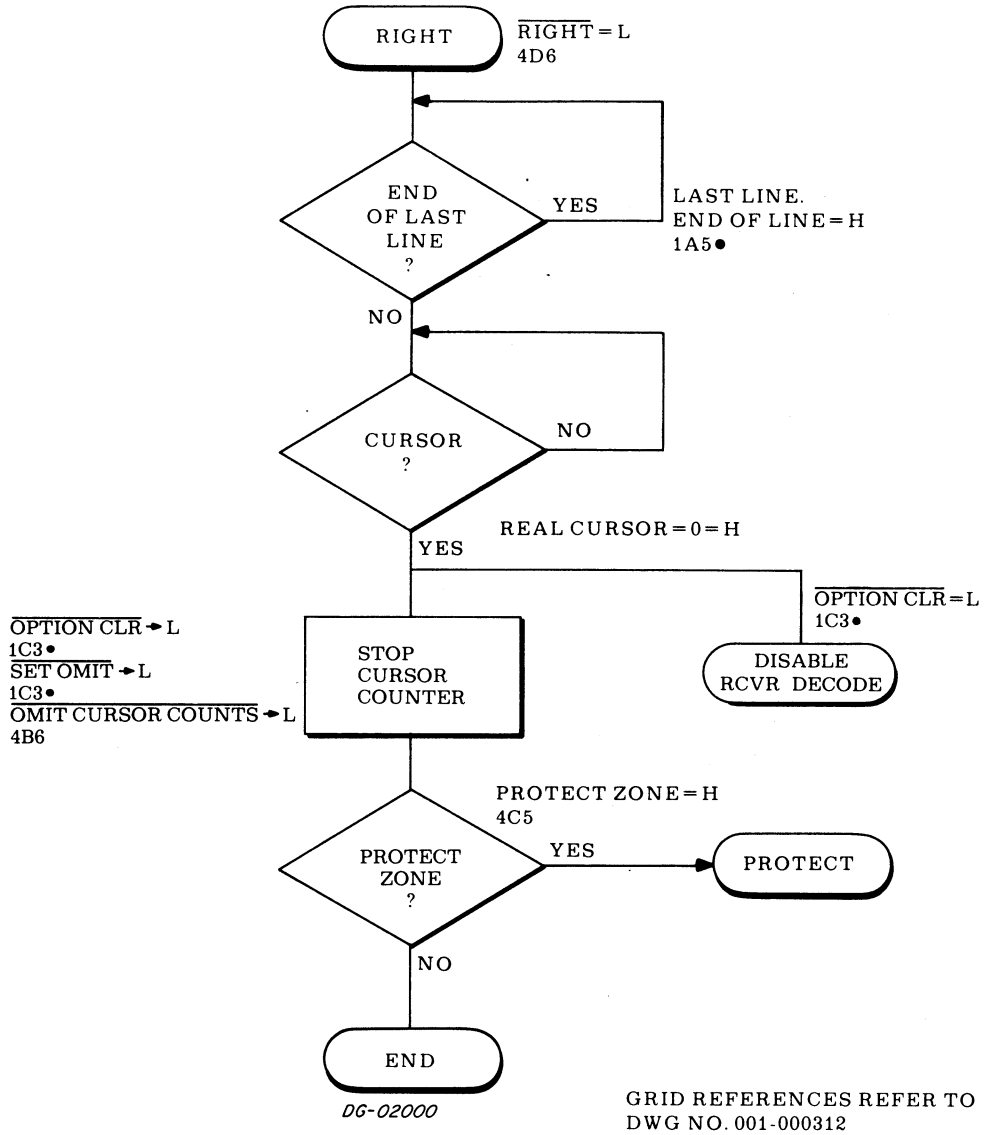
Implementation- Left is implemented by forcing an extra count into the cursor position indicator causing it to overflow one character earlier, effectively moving it left one position. The first bit in the cursor counter is frozen and the second bit is toggled when the signal "DOUBLE" is asserted. Left will not be implemented if the cursor is in the first character of the last line while in Roll mode, or if the cursor is at the first character of the first line in Page or Page-Buffered modes.



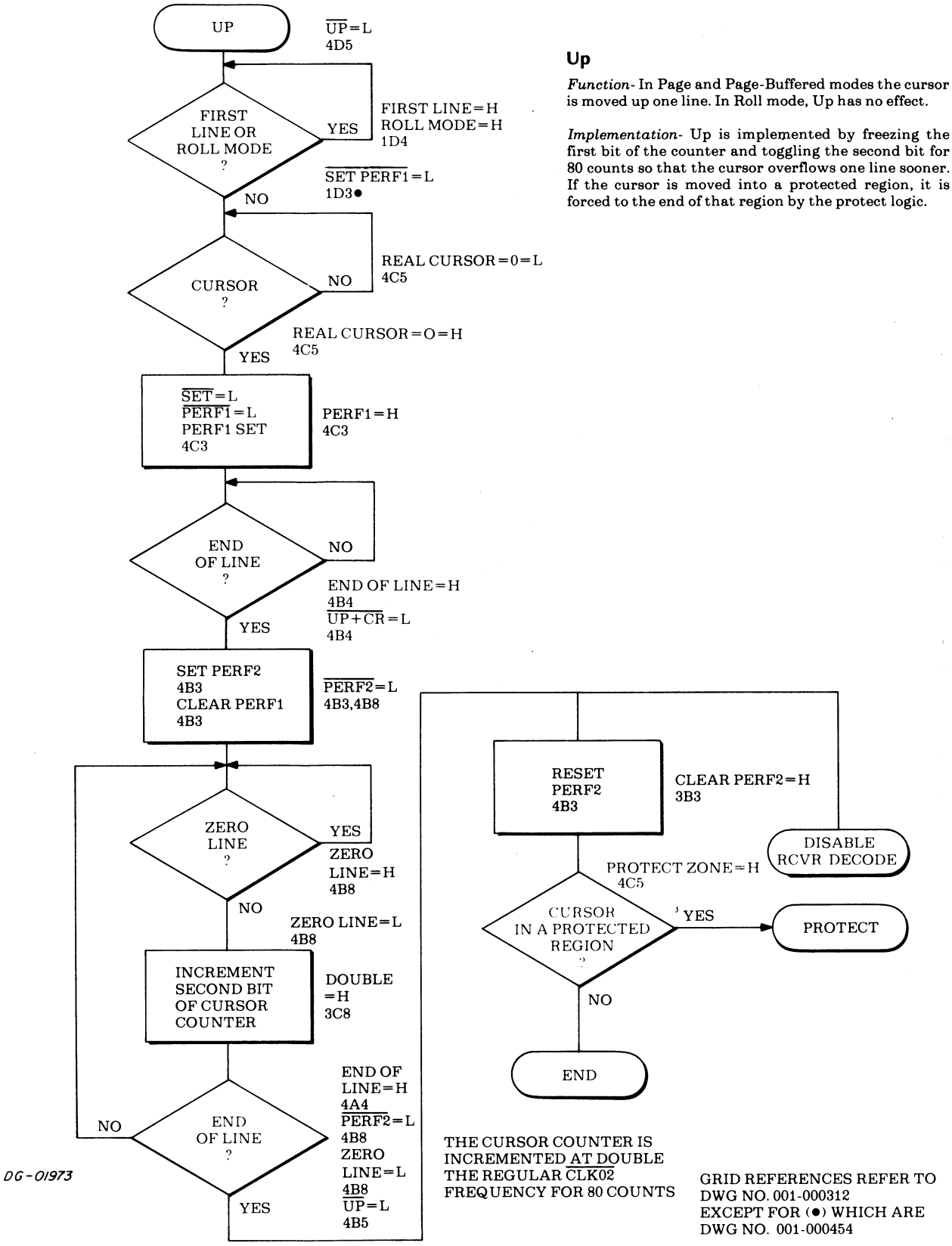
Right

Function- Moves the cursor right one character position.

Implementation- Cursor right simply deprives the cursor position indicator of one count so that it overflows one character position later, effectively moving it to the right. The actual implementation occurs just after overflow of the counter by stopping it for one clock period. If the cursor moves into a protected region, the cursor is forced to the end of that region by the protect logic. If the cursor is positioned at the last character of the last line, the command is ignored.



GRID REFERENCES REFER TO DWG NO. 001-000312 EXCEPT FOR (●) WHICH ARE DWG NO. 001-000454



DG-01973

THE CURSOR COUNTER IS INCREMENTED AT DOUBLE THE REGULAR CLK02 FREQUENCY FOR 80 COUNTS

GRID REFERENCES REFER TO DWG NO. 001-000312 EXCEPT FOR (●) WHICH ARE DWG NO. 001-000454

Up

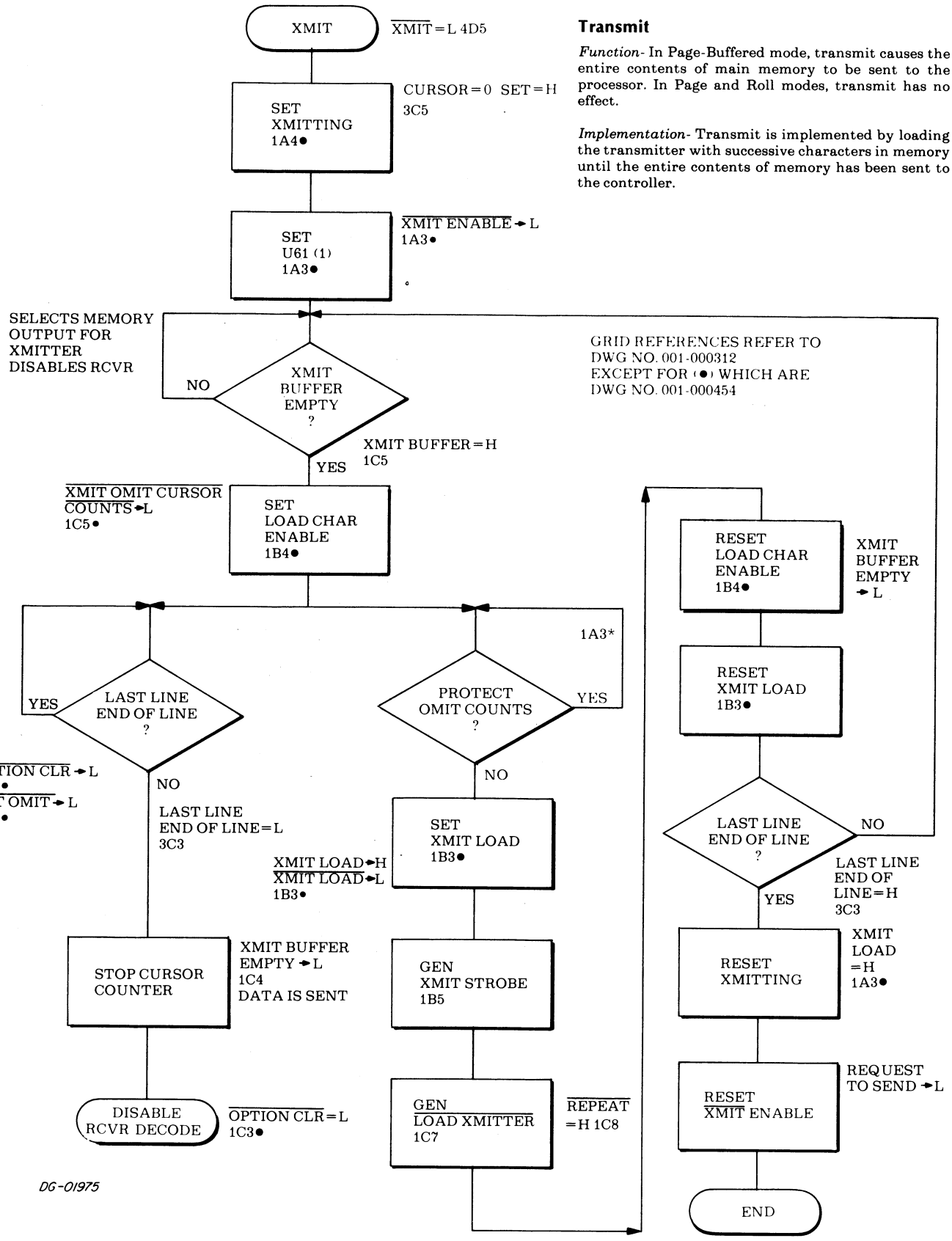
Function- In Page and Page-Buffered modes the cursor is moved up one line. In Roll mode, Up has no effect.

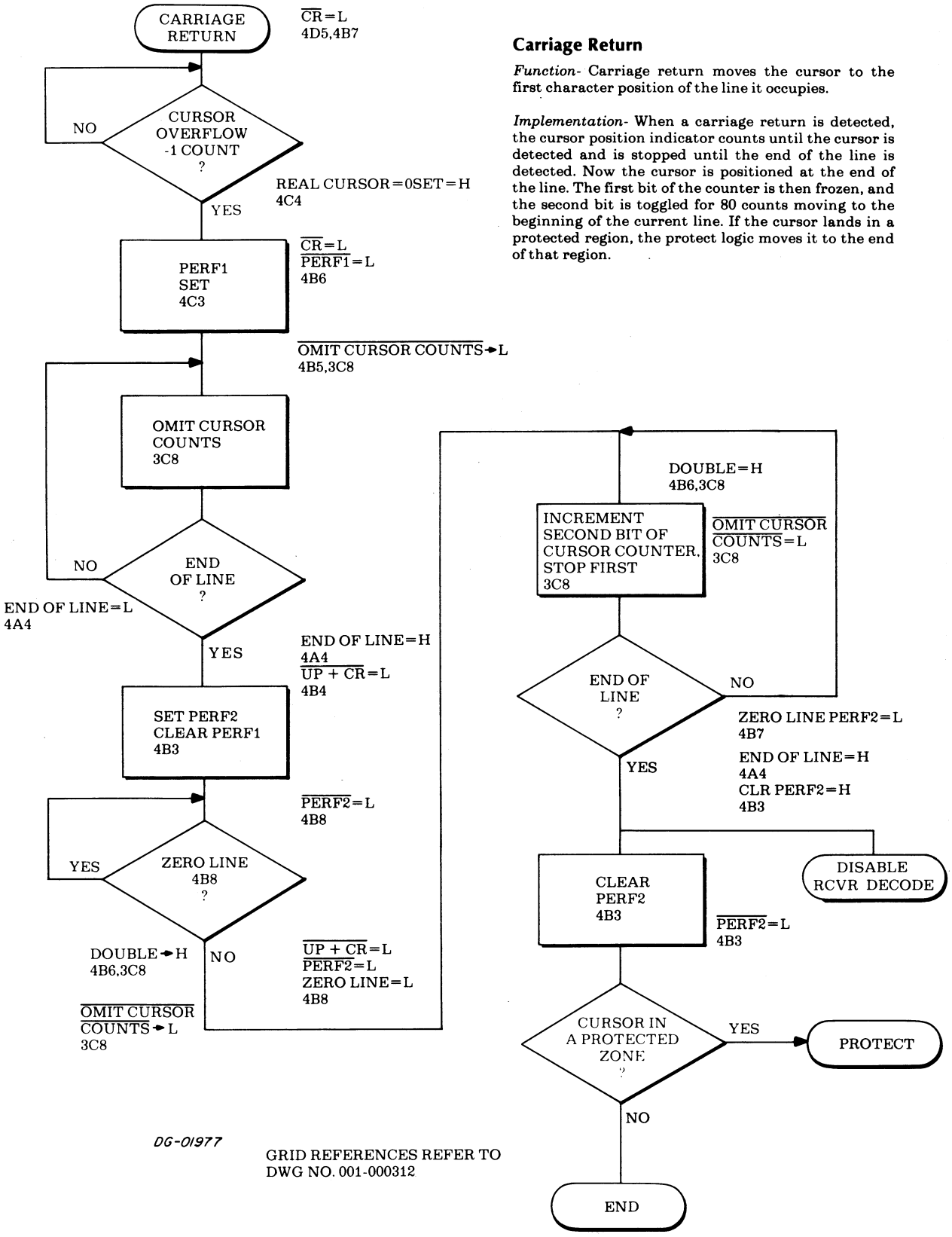
Implementation- Up is implemented by freezing the first bit of the counter and toggling the second bit for 80 counts so that the cursor overflows one line sooner. If the cursor is moved into a protected region, it is forced to the end of that region by the protect logic.

Transmit

Function- In Page-Buffered mode, transmit causes the entire contents of main memory to be sent to the processor. In Page and Roll modes, transmit has no effect.

Implementation- Transmit is implemented by loading the transmitter with successive characters in memory until the entire contents of memory has been sent to the controller.





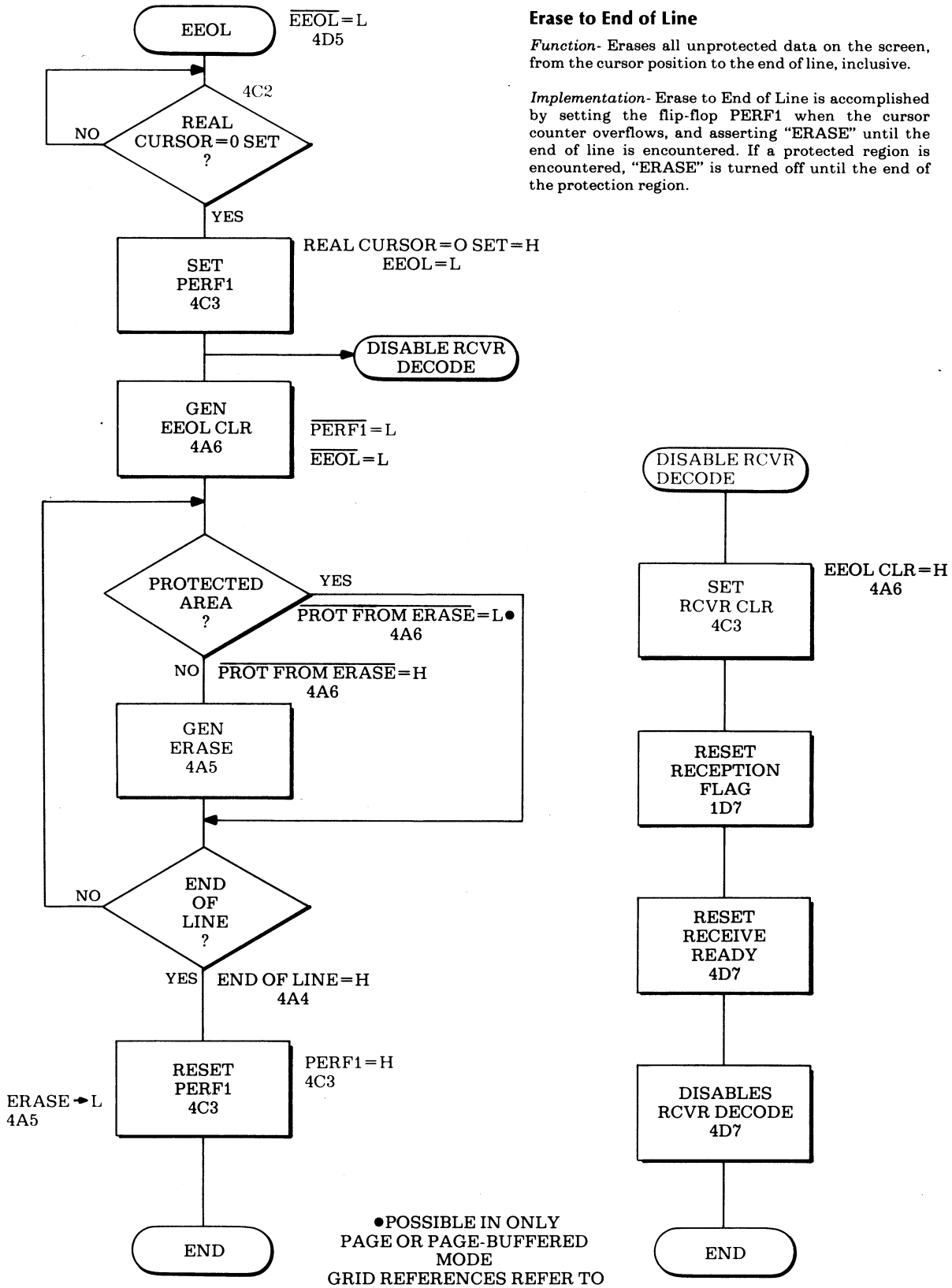
DG-01977

GRID REFERENCES REFER TO DWG NO. 001-000312

Carriage Return

Function- Carriage return moves the cursor to the first character position of the line it occupies.

Implementation- When a carriage return is detected, the cursor position indicator counts until the cursor is detected and is stopped until the end of the line is detected. Now the cursor is positioned at the end of the line. The first bit of the counter is then frozen, and the second bit is toggled for 80 counts moving to the beginning of the current line. If the cursor lands in a protected region, the protect logic moves it to the end of that region.



Erase to End of Line

Function- Erases all unprotected data on the screen, from the cursor position to the end of line, inclusive.

Implementation- Erase to End of Line is accomplished by setting the flip-flop PERF1 when the cursor counter overflows, and asserting "ERASE" until the end of line is encountered. If a protected region is encountered, "ERASE" is turned off until the end of the protection region.

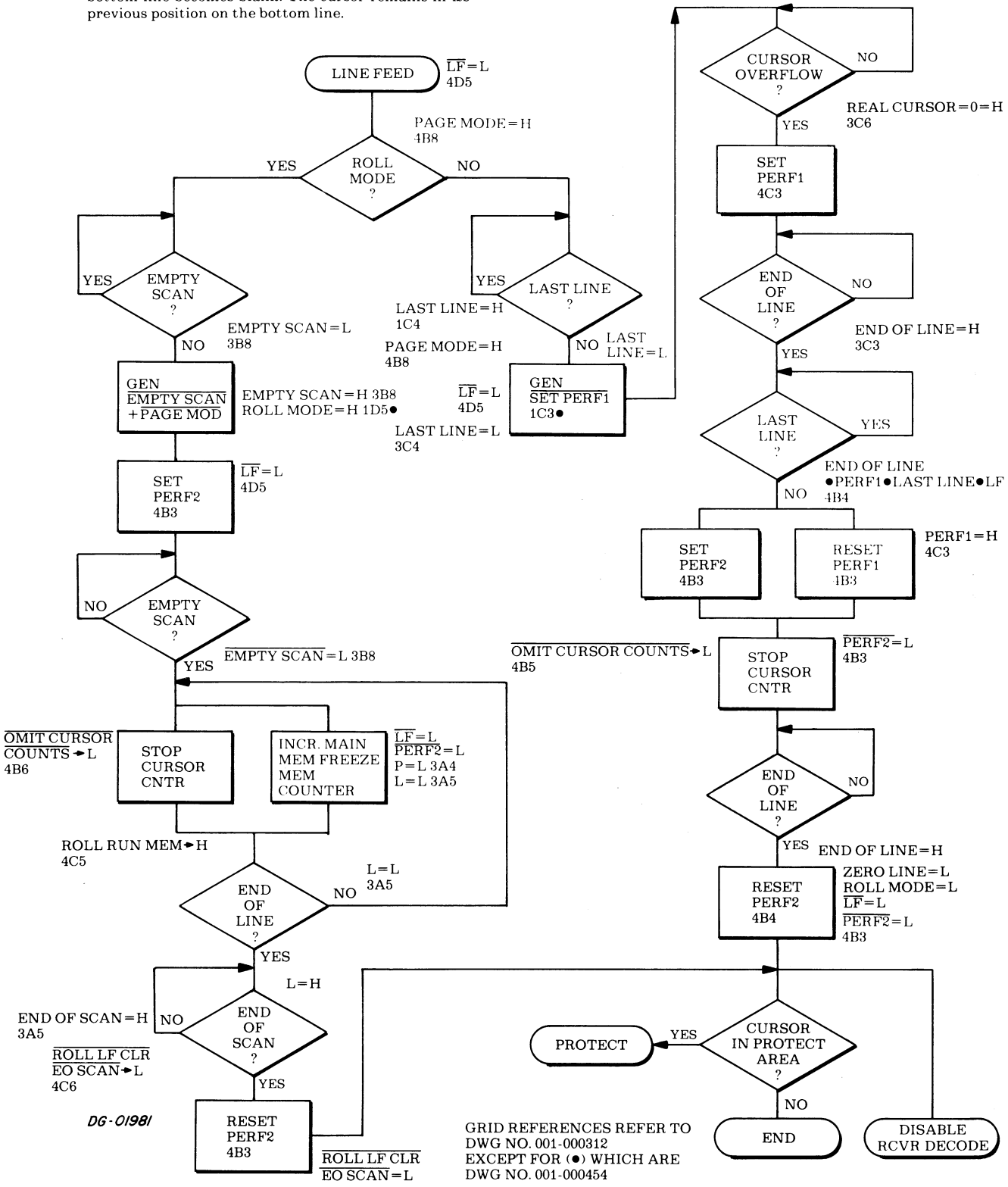
III

Line Feed

Function- In Page and Buffered modes, line feed moves the cursor down the screen one line. If the cursor is already on the bottom line, line feed has no effect.

In Roll mode, line feed moves all lines of data on the display screen up one line, losing the top line. The bottom line becomes blank. The cursor remains in its previous position on the bottom line.

Implementation- In Page and Page-Buffered modes, line feed is implemented by holding back 80 counts to the cursor counter after one "END OF LINE" signal and restarting it after the next. In Roll mode, line feed is implemented by incrementing the main memory during the tenth (empty) scan, and holding the cursor counter and main memory counter at their previous values.

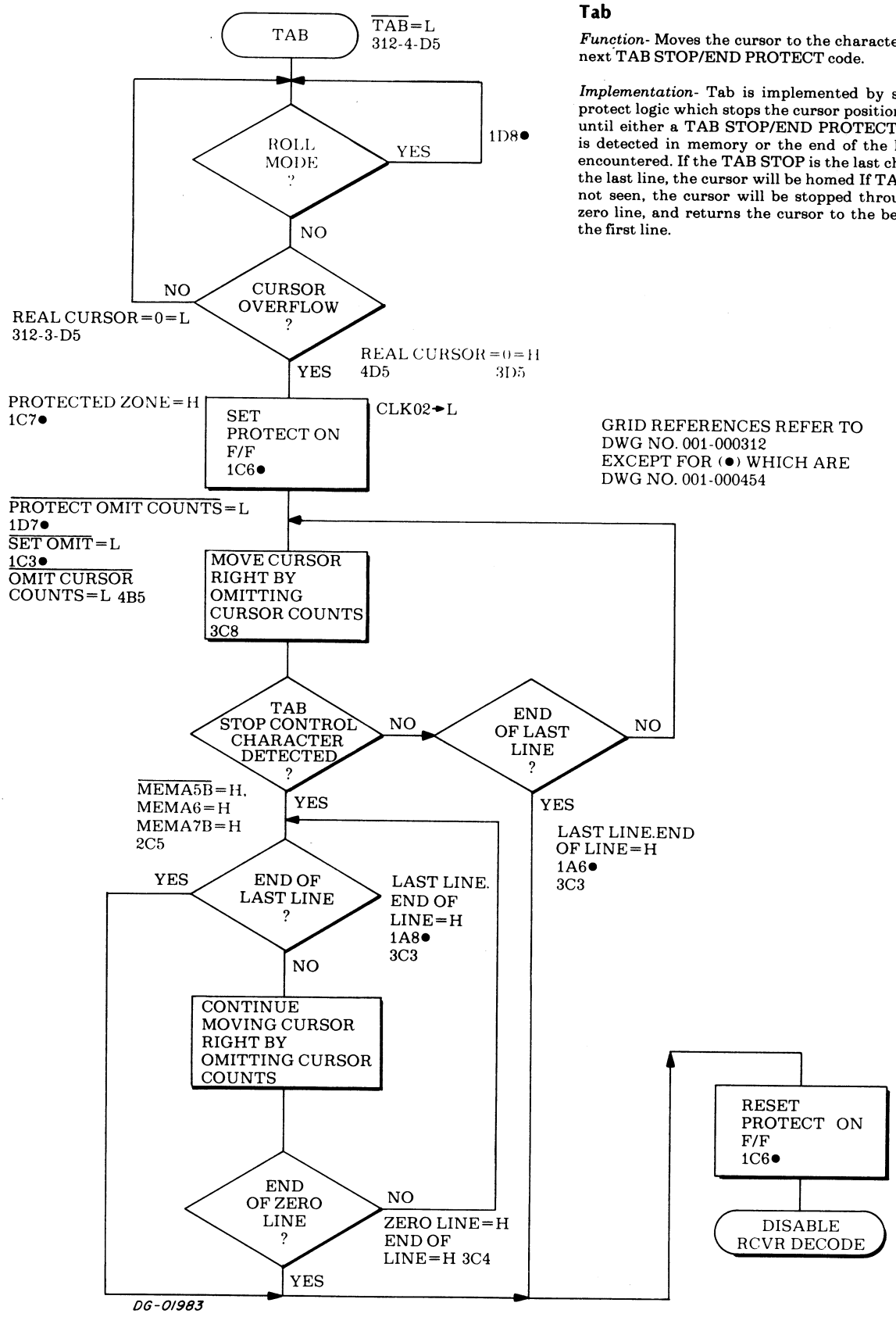


GRID REFERENCES REFER TO DWG NO. 001-000312 EXCEPT FOR (●) WHICH ARE DWG NO. 001-000454

Tab

Function- Moves the cursor to the character after the next TAB STOP/END PROTECT code.

Implementation- Tab is implemented by setting the protect logic which stops the cursor position indicator until either a TAB STOP/END PROTECT character is detected in memory or the end of the last line is encountered. If the TAB STOP is the last character in the last line, the cursor will be homed If TAB STOP is not seen, the cursor will be stopped throughout the zero line, and returns the cursor to the beginning of the first line.



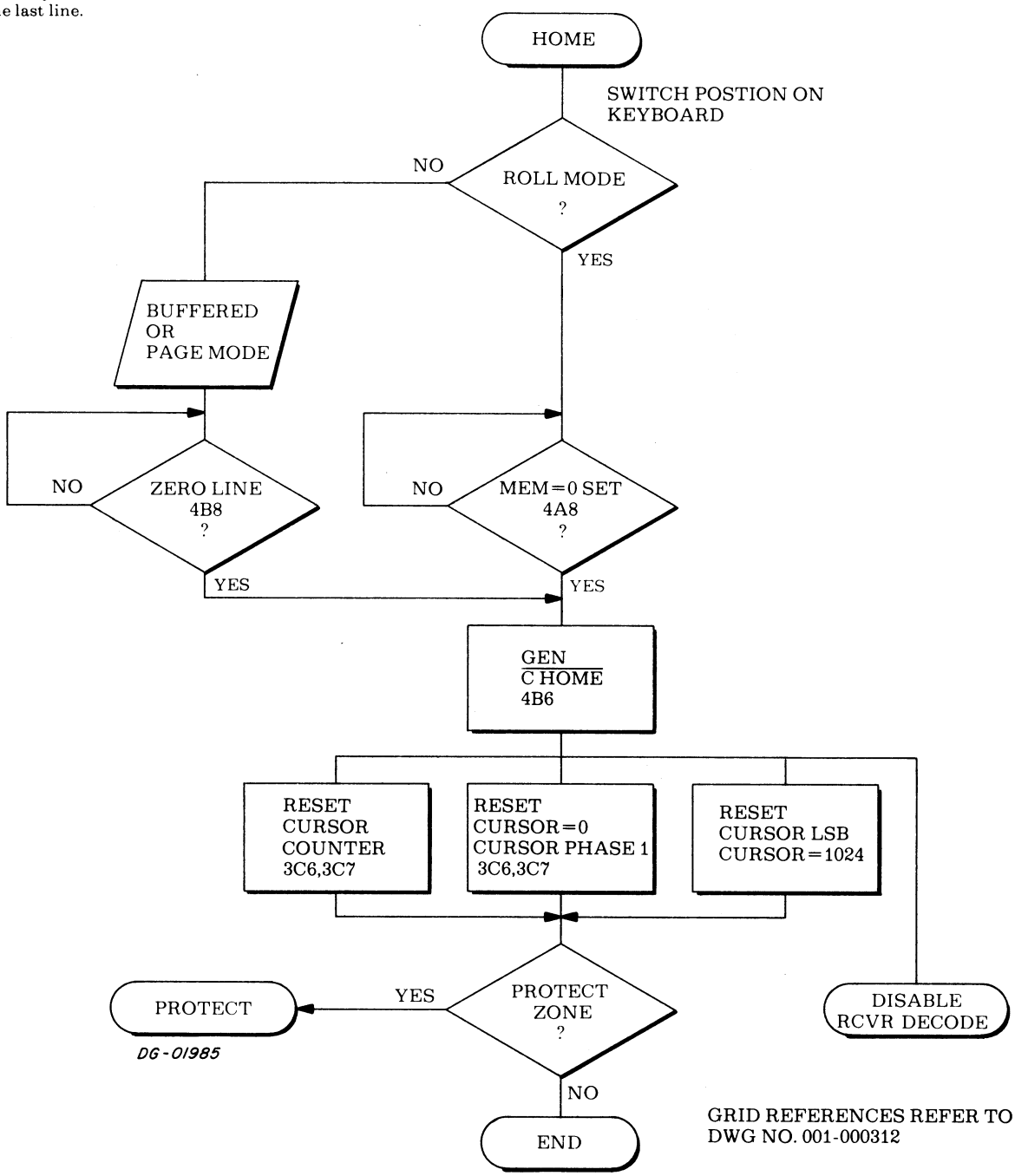
GRID REFERENCES REFER TO DWG NO. 001-000312 EXCEPT FOR (●) WHICH ARE DWG NO. 001-000454

Home

Function- In Page and Page-Buffered modes, home moves the cursor to the first character of the first line. In Roll mode, the cursor will be moved to the first character position of the last line.

Implementation- Page and Page-Buffered modes, home is implemented by waiting until "ZERO LINE" is asserted and then resetting the cursor position indicator, holding it until "FIRST LINE" is asserted.

In Roll mode, home is implemented by resetting the cursor position indicator at the point where the memory counter overflows, i.e., the first character of the last line.

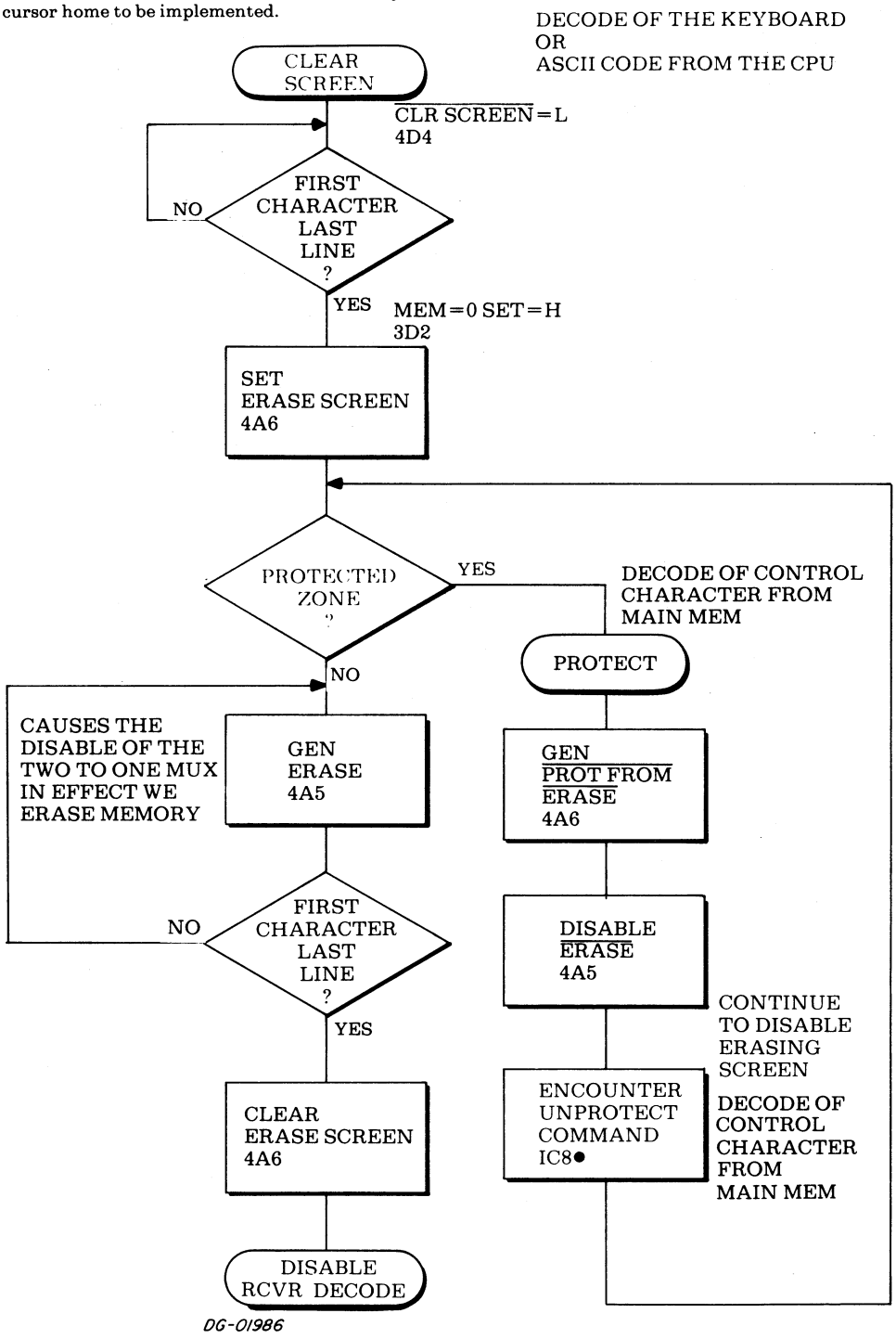


GRID REFERENCES REFER TO DWG NO. 001-000312

Clear Screen

Function- Erases all unprotected data on the screen and leaves the cursor in its home position.

Implementation- Sets "ERASE" between two successive first characters of last line, concurrently causing cursor home to be implemented.

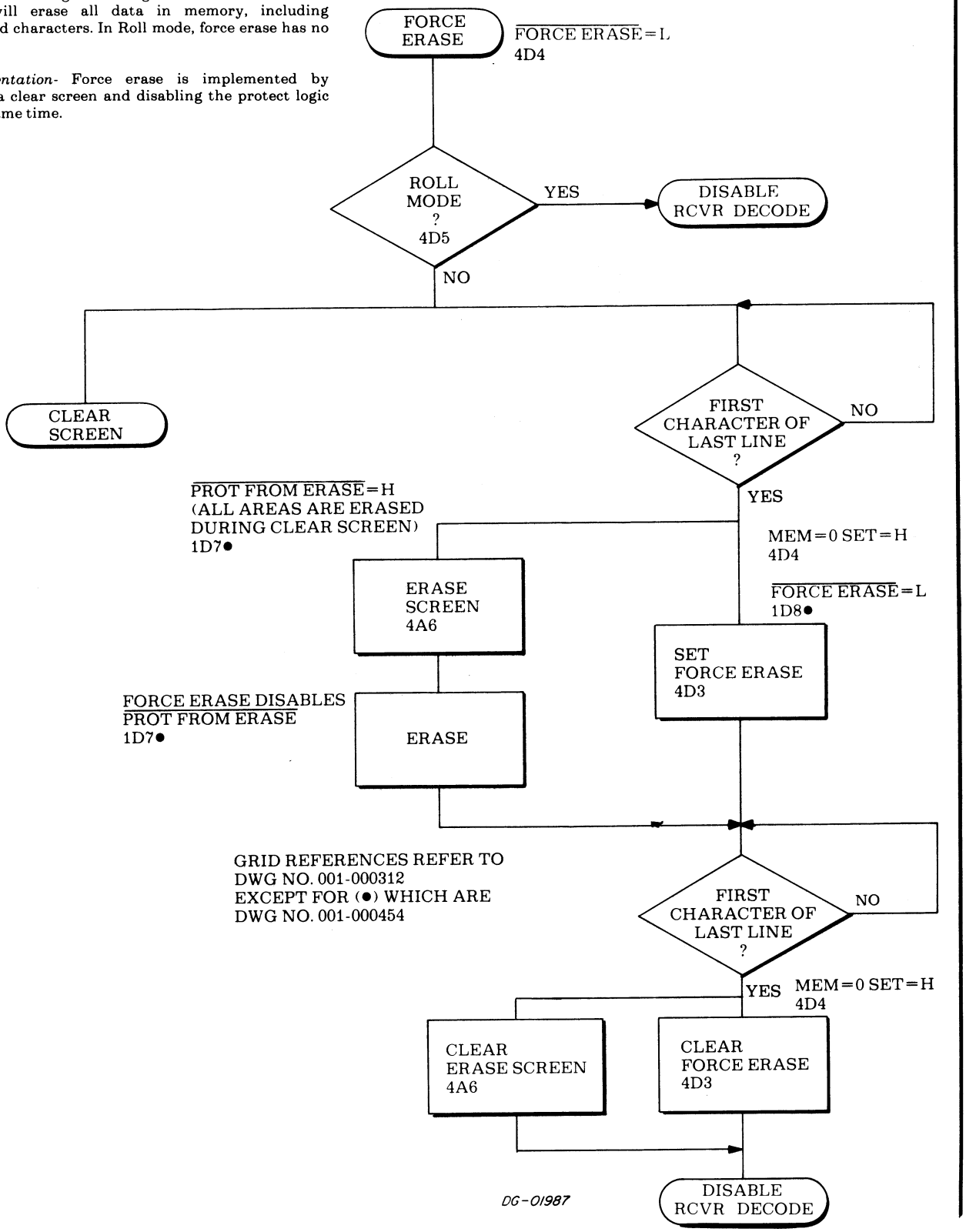


GRID REFERENCES REFER TO
DWG NO. 001-000312
EXCEPT FOR (●) WHICH ARE
DWG NO. 001-000454

Force Erase

Function- In Page and Page-Buffered modes, force erase will erase all data in memory, including protected characters. In Roll mode, force erase has no effect.

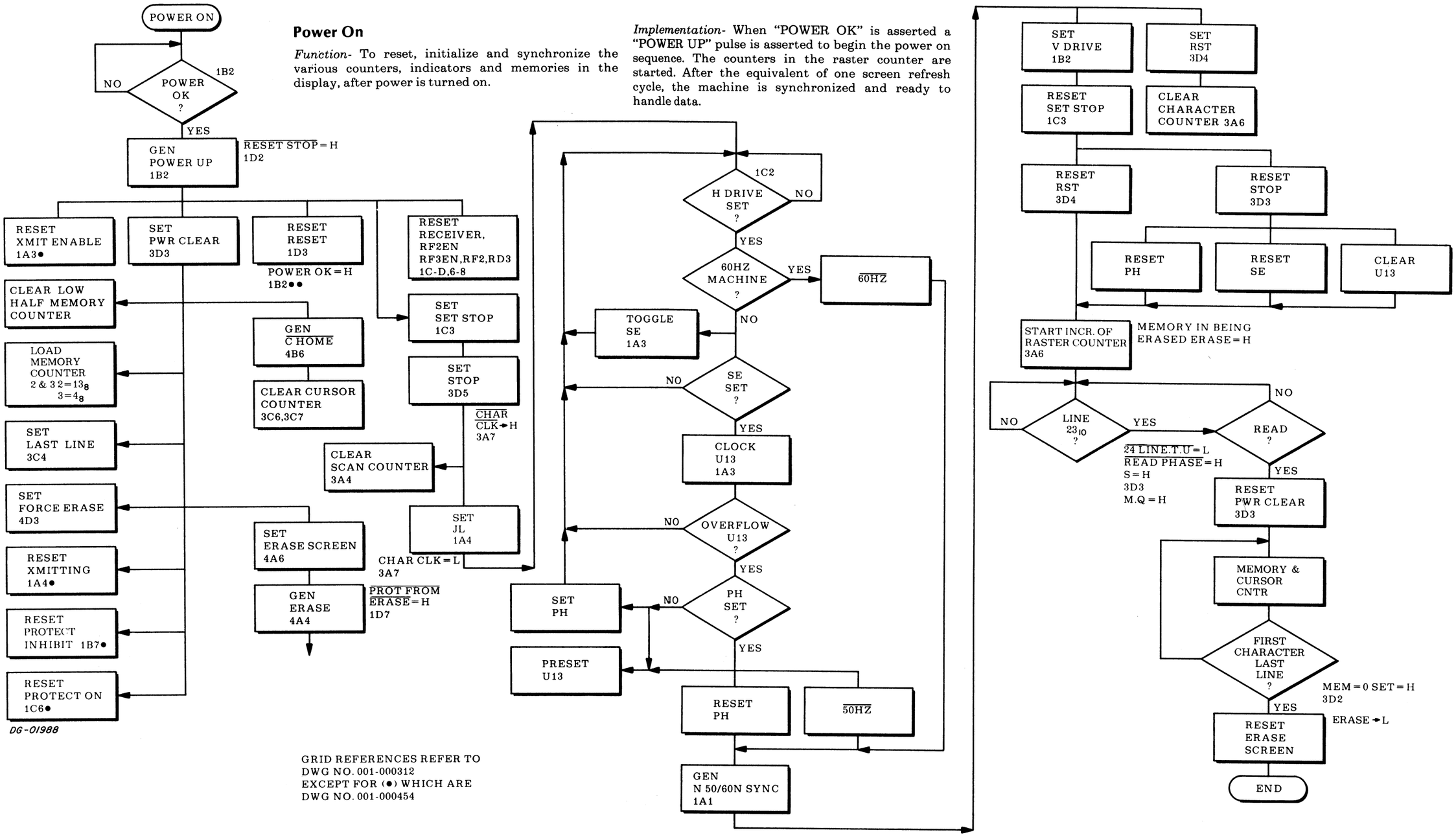
Implementation- Force erase is implemented by forcing a clear screen and disabling the protect logic at the same time.



Power On

Function- To reset, initialize and synchronize the various counters, indicators and memories in the display, after power is turned on.

Implementation- When "POWER OK" is asserted a "POWER UP" pulse is asserted to begin the power on sequence. The counters in the raster counter are started. After the equivalent of one screen refresh cycle, the machine is synchronized and ready to handle data.



GRID REFERENCES REFER TO
DWG NO. 001-000312
EXCEPT FOR (●) WHICH ARE
DWG NO. 001-000454

SECTION IV

THE DISPLAY INTERFACE

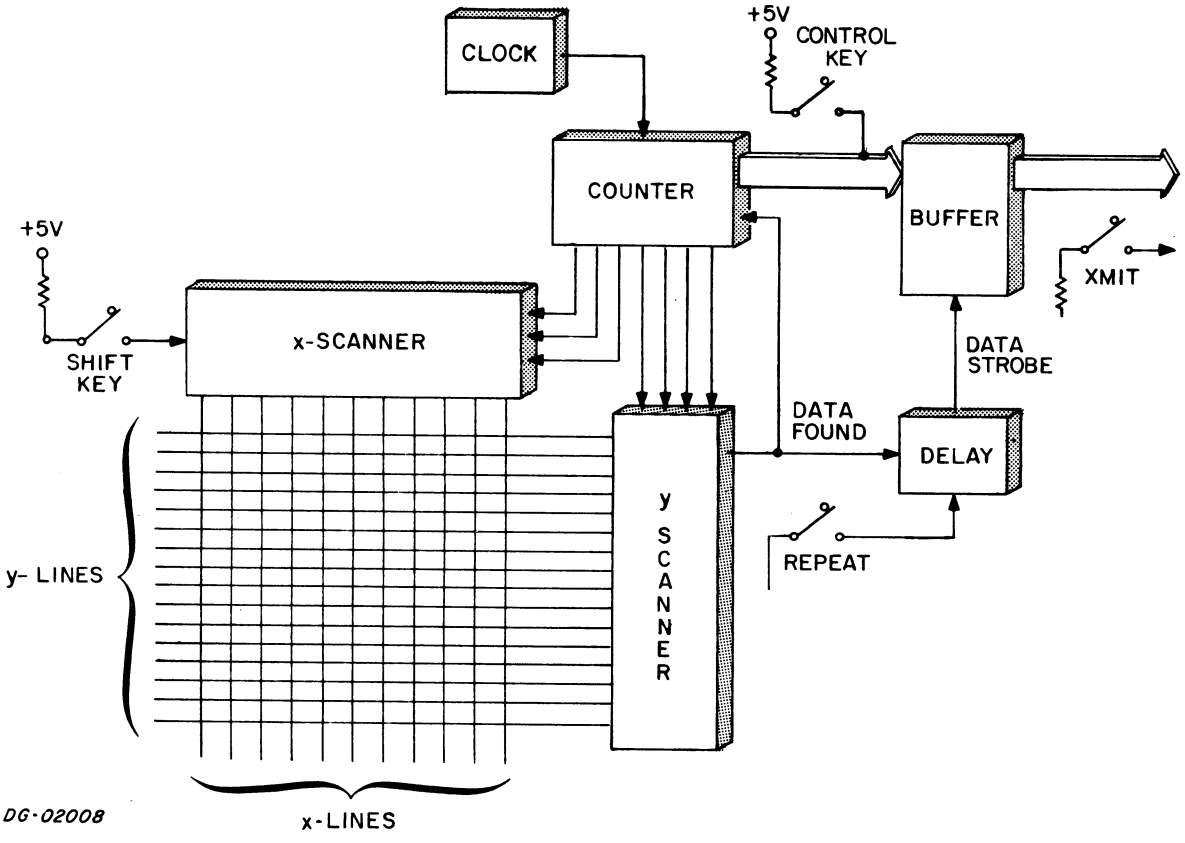
GENERAL

The display interface controls the flow of data between the display control, I/O controller, and the operator. It consists of a keyboard and a receiver/transmitter section. The keyboard provides a human interface, while the receiver/transmitter controls the actual data transfer.

THE KEYBOARD

The keyboard is a mechanically switched, 73 station, teletypewriter style TTL/ASCII encoded device. It uses four level decoding, and provides both interlock and two key rollover features. Appendix B lists the character codes generated by the keyboard.

KEYBOARD BLOCK DIAGRAM



The keyboard is organized as shown above. Each key is wired to an x and y-line at intersecting points (nodes) on the array of signal lines. When a key is depressed, its x- and y- line come into contact. A 7-bit counter causes the scanner to sequentially check each node on the array for a completed circuit, by forcing a low voltage level on the x-line, and searching for a low voltage on the corresponding y-line. When the scanner detects a node with a depressed key, this is called a "hit". When such a hit occurs, the scanner pauses and the appropriate ASCII code for that key is generated. The scanner can address all nodes in about 13ms (a typing speed of about 900wpm is required for a keystroke to be missed).

The scanner selects each node to be checked from the value of the seven bit counter and the state of the shift key. The value of the three high order bits of the counter and shift key select one of the eleven x-lines, and the value of the four low order bits of the counter select one of the sixteen y-lines. The nodes of the keyboard scanning array are arranged so that the counter value selecting each node equals the ASCII code for the alphanumeric character assigned to the key at that node. When the shift key is depressed, certain nodes are selected by a different value of the counter and consequently generate a different code. Thus, when the scanner makes a hit and pause, the value of the counter is placed on the output lines, a strobe pulse asserts and the appropriate ASCII code for the character is sent to the transmitter.

The control key generates control codes from the corresponding alphanumeric codes whenever it is depressed. This is possible since control codes differ from the alphanumeric code only in the high order bit position. Thus, the action of the control key is to force the high order bit of the character code to 0.

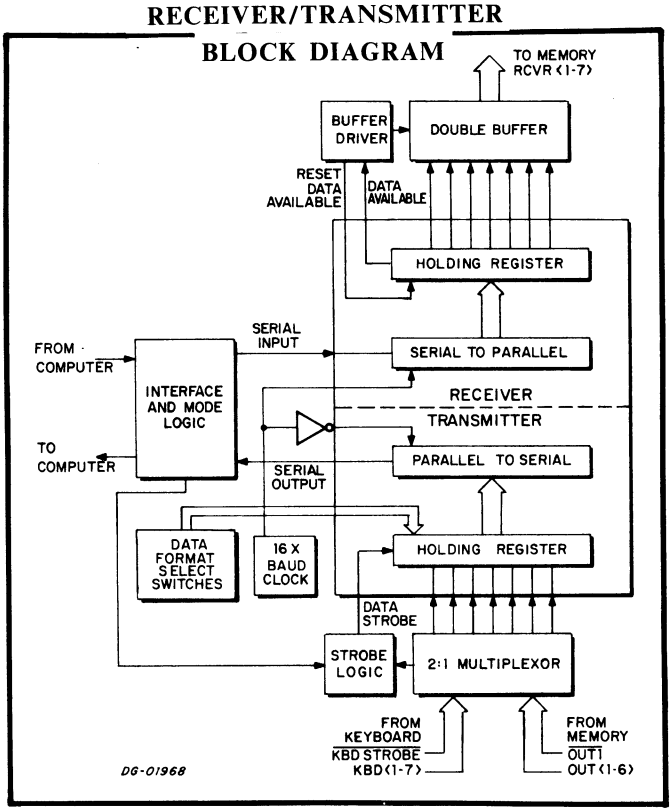
The repeat key provides a repeating strobe for the output lines. The scanner remains stopped, and the strobing pulse continues until either the character key or the repeat key is released.

The interlock and rollover features govern the operation of the keyboard when two keys are depressed. When one key is depressed and a second is then depressed, the code for the second key will not be generated (interlock). Upon release of the first key, the code for the second key is generated (rollover) provided it remains depressed.

THE RECEIVER/TRANSMITTER

The receiver/transmitter in the display is the interface to the data controller in the computer. There are many different types of controllers which operate using different codes. By changing switch configurations on the display control board, the receiver/transmitter is able to interface to many of these controllers. It is based on an LSI subsystem asynchronous receiver/transmitter integrated circuit (UART), DGC part number 100-000130/536. The UART receives serial data and converts it to parallel data for use in the display, and converts parallel data to serial data to be transmitted to the computer. Associated with the UART are the interface logic, a keyboard/memory data multiplexor, a double buffer, and a data clock.

RECEIVER/TRANSMITTER
BLOCK DIAGRAM



The receiver/transmitter unit is designed to be interfaced to 20ma and 60ma current loop as well as EIA type interfaces. The interface type and full- or half-duplex operation are selected through switches on the display PC board all external to the chip. These switches modify the data path within the interface logic to accept the type of interface desired.

A data clock controls the baud rate of the receiver/transmitter unit. The UART may operate at any baud rate but DGC restricts the selection to certain speeds from 110 to 4800 baud. The baud rate is selected through switches.

Data from the I/O controller is accepted at the interface logic in serial form, and is sent to the UART to be stripped of any Stop Start and Parity bits (preselected by switches), and changed to parallel form for use in the display control logic. When the UART is loaded, a strobing pulse asserts, the data is clocked into the double buffer, and then sent to the display control logic. to be decoded.

To send data from the keyboard or display control logic, a multiplexor loads the UART with the data in parallel form. The data is then changed to the switch selected code format and shifted to the interface logic serially. The interface logic converts the signals to the proper levels for the interface being used. In half-duplex mode the output of the transmitter section of the UART is also looped around to the receiver section, so characters are sent to both the computer and the display control logic.

Data Protocol

Certain protocols defining data flow exist between the receiver/transmitter, the keyboard, the I/O controller, and display control. These protocols are dependent upon the three modes of display operation; Page-Buffered, Page, and Roll.

In Page-Buffered mode, the transmitter accepts data from keyboard, and sends it directly to the receiver, and consequently on to the display control. Only when a transmit control is given, will data be sent to the I/O controller. When this occurs, the entire contents of main memory is sent to the I/O controller. The receiver can accept data from the controller at any time, inserting it into main memory.

In Page and in Roll modes, data from the keyboard is sent to the I/O controller directly, and depending upon the selection of full- or half-duplex operation, it may be sent to the display control also. The difference between Page and Roll mode lies in the ability to control the cursor. In Page mode, the cursor may be positioned anywhere on the screen while in Roll mode, the cursor is limited to the bottom line. Thus Roll mode allows access only to the line presently being typed.

REFERENCES

1. Schematic- Keytronix Keyboard 035-0998

2. Components Guide 015-000028-02

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SECTION V

THE DISPLAY POWER SUPPLY

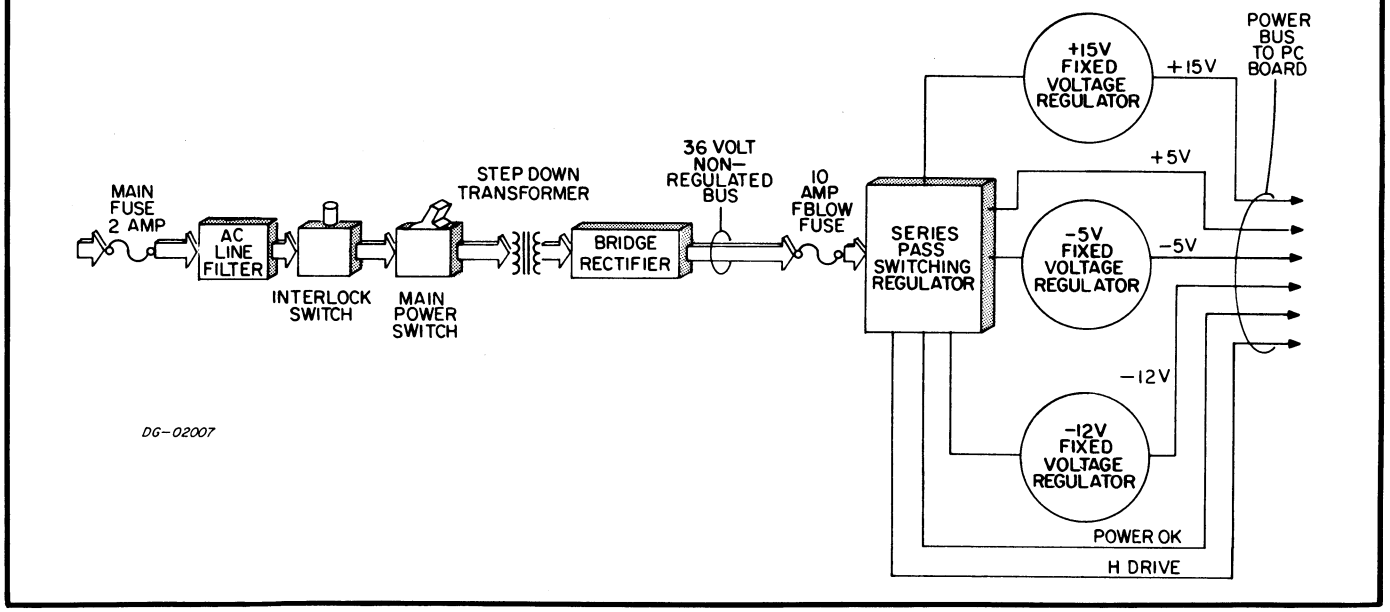
GENERAL

The 6012 display power supply converts ac power (120Vac, 50 or 60Hz) to the required dc power at low voltage, necessary for the logic circuits and the monitor. There are four low output voltages from the main supply, summarized in the following table.

Voltage	Maximum Current
+15Vdc	1.0 Amps
+ 5Vdc	3.9 Amps
- 5Vdc	300 mA
-12Vdc	400 mA

The power supply is a module mounted on the monitor chassis, and is cabled to the display through a connector. 120Vac or 220Vac is input from a three prong plug and power cord to a 2amp line fuse. Power passes from the fuse to an interlock switch on the display chassis, and on to the transformer. The transformer is mounted separate from the power supply module, on the main chassis. The primaries of the transformer are wired in parallel for 110Vac operation and in series for 220Vac operation. The secondaries of the transformer are wired to a full-wave bridge rectifier which outputs +36Vdc non-regulated. The +36VNR is wired to a 10amp fuse and a crowbar circuit for overvoltage protection and is used by the series pass switching regulator which controls the +15Vdc, +5Vdc, -5Vdc, and -12Vdc supplies. The following figure illustrates the power supply and its major components.

POWER SUPPLY BLOCK DIAGRAM



THE REGULATORS

There are two types of voltage regulators in the display power supply. The first is a series pass switching regulator which controls the +5Vdc supply directly, and controls the regulators for the other low voltage supplies. The second are three fixed voltage regulators which use power derived from the switching regulator to regulate the +15Vdc, and -12Vdc supplies.

The Series Pass Switching Regulator

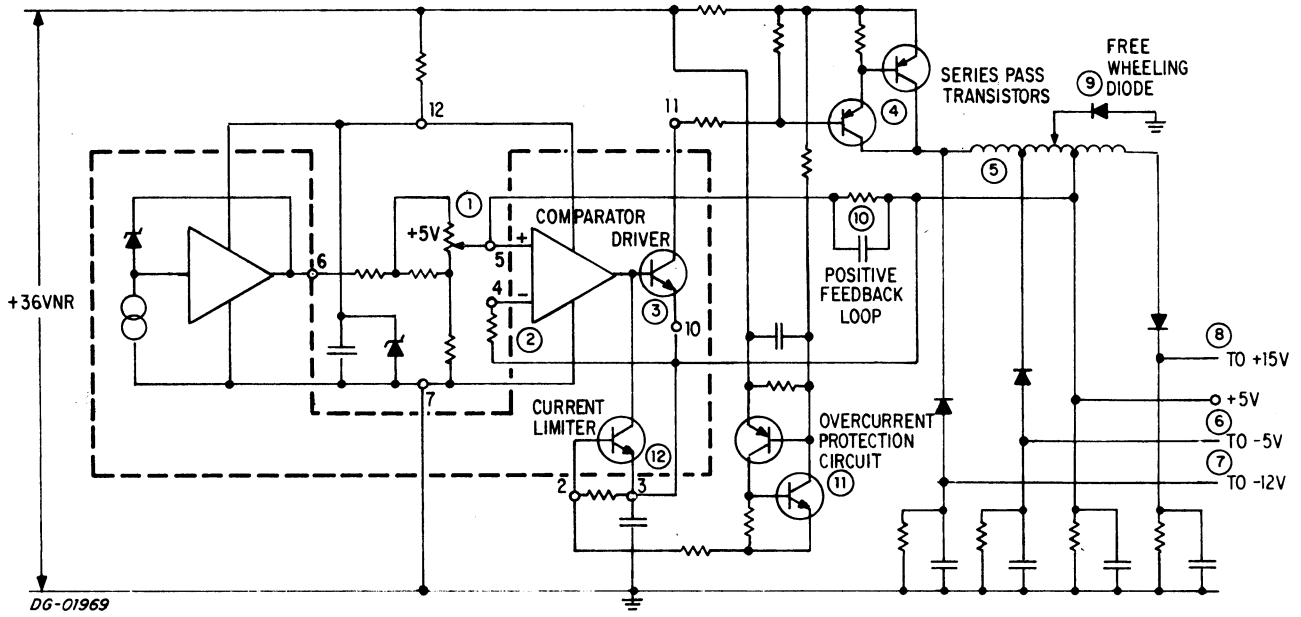
The regulator operates in the following manner:

When the comparator senses a difference between the (divided) reference voltage (1) and the output (2), it switches, turning on the driver transistor (3) and the series pass transistors (4). Current is shunted through the series pass transistors to the coil, output capacitor, and +5V load (5). The voltage rises, reducing the error voltage to the comparator which resets, turning off the driver (3) and consequently the series pass transistors. Now the power is supplied from the power stored in the LC circuit. The back emf developed across the coil as a result of this switching is used to power the -12V and -5V fixed voltage regulators (6) (7). Since the voltage across the coil will be as high as +15V, the +15V fixed voltage regulator is also fed from the coil. Excess emf across the coil is dropped across the free wheeling diode (9). Note that each time the comparator is forced to switch, it is driven into saturation by the positive feedback loop (10).

The overcurrent protector circuit (11) will turn the current limited (12) on if the series pass transistors draw too much current. It senses the voltage on the emitter of the final series pass transistor, and if it drops too low, the current limiter (12) is turned on. Subsequently, the driver and the series pass transistors are turned off. The current limiter remains latched in this state until power is removed and then restored. Note that should the +5V rise too high, the zener diode in the crowbar circuit triggers and SCR which shorts the unregulated supply to ground, blowing fuse F1.

The following is a simplified schematic of the series pass switching regulator:

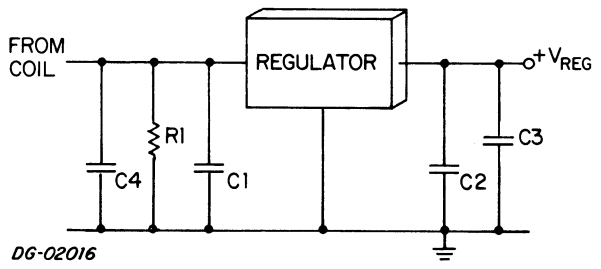
SERIES PASS SWITCHING REGULATOR SCHEMATIC



The Fixed Voltage Regulators

The following is a schematic of the external circuitry associated with the fixed voltage regulator:

FIXED VOLTAGE REGULATOR SCHEMATIC

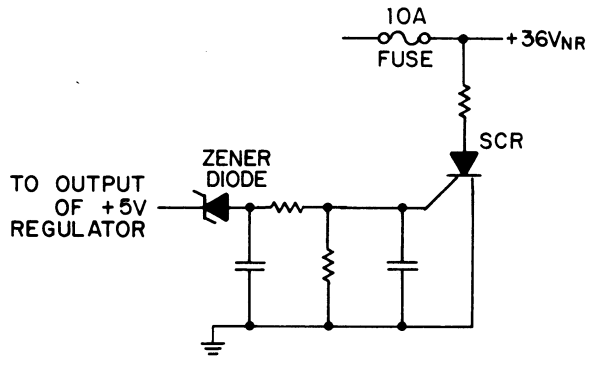


Capacitor C1 is necessary as a filter on the input stage, C2 and C3 are necessary to improve the transient response of the circuit. C4 and R1 combined with the coil, provide the power to the regulator.

OVERVOLTAGE PROTECTION

The power supply is monitored at the output of the +5Vdc regulator for overvoltage conditions. If the voltage at this point rises above a safe limit, a crowbar circuit shorts the +36Vdc level to ground and causes the 10amp fuse F1 to blow. An SCR is used to shunt the +36Vdc supply to ground. The monitor circuit for the +5Vdc regulator and the SCR "fuse popping" circuit is shown below.

OVERVOLTAGE PROTECTION SCHEMATIC



OVERCURRENT PROTECTION

An overcurrent protection circuit improves the response at the current limiting transistor internal to the switching regulator. If the load on the +5V supply should become too much, then this circuit shunts current from the two series pass transistors in the supply and turns off the current switching (driver) transistor, which in turn switches off the series pass transistors in the regulator. The protector also shunts current surges at power up, protecting the logic from burn out. The constant voltage regulators for the +15V, +5V, and -12V supplies also contain their own internal current limiters.

FUSES

There are two fuses in the 6012 power supply, an AC line fuse and a DC fuse. The line fuse is located on the rear panel of the display, a 2amp slow blow for 110Vac, or a 2amp fast blow for 220Vac operation. The DC fuse is a 10amp fast blow, located on the power supply module printed circuit board.

LOGIC SIGNALS

Two logic signals are developed in or used by the power supply, POWER OK and HDRIVE. POWER OK is used to initiate the power up operation, and HDRIVE is a feedback to the horizontal drive circuitry to prevent screen roll and flutter.

V

REFERENCES

1. Print- Display Power Supply 001-000648-05

2. National Linear Integrated Circuits Catalog, June 1973

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APPENDIX A

THE DGC 6012 DISPLAY SPECIFICATIONS

PROPERTIES	
Mounting	Tabletop, 13 x 18 1/4 x 23 3/4 inches
Weight	35 pounds
Operating Temperature Range	5° to 45° Centigrade
Operating Humidity Range	10% to 95% non-condensing
Power Requirements	100-130Vac, single phase 60Hz ±5% 1.2A, 140 watts or 100-130Vac, single phase 50Hz ±5% 1.2A, 140 watts or 200-269Vac, single phase 50Hz ±5% .6A, 140 watts
SYSTEM CAPACITY	
Number of displays/system	Depends on controller
Display Information Capacity	1920 characters, formatted as 24 lines, 80 characters/line displayed in a 6 by 9 inch area on a 12 inch CRT
CHARACTERISTICS	
Data Transmission Mode	Serial, bit by bit, character by character, lower order bit transmitted first. Full- or half-duplex, user selectable
Code Format	ASCII; 10 or 11-bit, user selectable Even, or odd, user selectable at the terminal
Interface	20mA current loop 60mA current loop EIA - RS-232C
Keyboard Codes	98 seven-bit codes plus a parity bit
Display Codes	64 seven-bit codes plus a parity bit which is ignored by the terminal. Letters are upper case only; lower case will be displayed as upper case
Character Transfer Rate	User selectable: 110, 150, 300, 600 1200, 1800, 2400, 3600, or 4800 baud limited by controller in use.
Screen Fill Time	4 sec. @ 4800 baud to 3 min. @ 110 baud.

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APPENDIX B

ASCII CHARACTER CODES

Name	Symbol Display	7-Bit Octal Code	Key	
			Main Keyboard	Suppl. Keyboard
Space	Non Printing	040	Space Bar	-
Exclamation Mark	!	041	SH 1	-
Quotation Marks	"	042	SH 2	-
Number Sign	#	043	SH 3	-
Dollar Sign	$	044	SH 4	-
Percent	%	045	SH 5	-
Ampersand	&	046	SH 6	-
Apostrophe	'	047	SH 7	-
Opening Parenthesis	(	050	SH 8	-
Closing Parenthesis	)	051	SH 9	-
Asterisk	*	052	SH :	-
Plus	+	053	SH ;	-
Comma	,	054	,	-
Hyphen (Minus)	-	055	-	-
Period (Decimal Point)	.	056	.	-
Slant	/	057	/	-
Zero	0	060	0	0
One	1	061	1	1
Two	2	062	2	2
Three	3	063	3	3
Four	4	064	4	4
Five	5	065	5	5
Six	6	066	6	6
Seven	7	067	7	7
Eight	8	070	8	8
Nine	9	071	9	9
Colon	:	072	:	-
Semicolon	;	073	;	-
Less Than	<	074	SH ,	-
Equals	=	075	SH -	-
Greater Than	>	076	SH .	-
Question Mark	?	077	SH /	-
Commercial At	@	100 (140)	SH P	-
A	A	101 (141)	A, SH A	-
B	B	102 (142)	B, SH B	-
C	C	103 (143)	C, SH C	-
D	D	104 (144)	D, SH D	-
E	E	105 (145)	E, SH E	-
F	F	106 (146)	F, SH F	-
G	G	107 (147)	G, SH G	-
H	H	110 (150)	H, SH H	-
I	I	111 (151)	I, SH I	-
J	J	112 (152)	J, SH J	-
K	K	113 (153)	K,	-
L	L	114 (154)	L,	-
M	M	115 (155)	M,	-
N	N	116 (156)	N,	-
O	O	117 (157)	O,	-
P	P	120 (160)	P,	-
Q	Q	121 (161)	Q, SH Q	-
R	R	122 (162)	R, SH R	-
S	S	123 (163)	S, SH S	-
T	T	124 (164)	T, SH T	-
U	U	125 (165)	U, SH U	-
V	V	126 (166)	V, SH V	-
W	W	127 (167)	W, SH W	-
X	X	130 (170)	X, SH X	-
Y	Y	131 (171)	Y, SH Y	-
Z	Z	132 (172)	Z, SH Z	-
Opening Bracket	[	133 (173)	SH K	-
Reverse Slant	\	134 (174)	SH L	-
Closing Bracket	]	135 (175)	SH M	-
Circumflex	^	136 (176)	SH N	-
Underline	—	137 (177)	SH O	-

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Lower case are displayed as upper case
Bracketed codes are not generated by the Keyboard but are displayed as their unbracketed equivalents.

APPENDIX B (Continued)

CONTROL CHARACTERS

Name	Octal Code	Main Keyboard	Supplementary Keyboard	Function*
HOME	010	CTRL H	HOME	Moves cursor to first unprotected position on the screen
TAB	011	CTRL I	TAB	Moves cursor to position following the first unprotected TAB STOP/END protect character to the first unprotected end character
LINE FEED	012	LINE FEED or CTRL J	↓	Moves cursor down one line
CLEAR TO END OF LINE	013	CTRL K	CLEAR EOL	Erases unprotected data to end of line. Cursor does not move
CLEAR	014	CTRL L	CLEAR	Clears all unprotected data on screen and moves cursor to first unprotected position on the screen
CARRIAGE RETURN	015	RETURN or CTRL M	-	Moves cursor to first unprotected position in its line
TRANSMIT BUFFER	016	CTRL N	-	Transmits the unprotected contents of terminal's memory from cursor position to the end of the page
CURSOR UP	017	CTRL 0	C↑	Moves the cursor up one line
CURSOR RIGHT	030	CTRL X	C→	Moves the cursor right one position
CURSOR LEFT	031	CTRL Y	C←	Moves the cursor left one position
FORCE ERASE	034	CTRL SHIFT L	-	Erases all protected and unprotected data on the screen
TAB STOP/END PROTECT	035	CTRL SHIFT M	-	Is both a Tab Stop and the end delimiter of a protect zone
START PROTECT	036	CTRL SHIFT N	-	Is the starting delimiter of a protected zone
BLINK	037	CTRL SHIFT O	-	Delimits a blinking zone
MASTER RESET	-	CTRL RESET	-	Simulates power on synchronization sequence

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*NOTE: See Section on COMMANDS for details

APPENDIX B (Continued)

PROTOCOL CHARACTERS

Name	Standard Mnemonics	Octal Code	Key	
			Main Keyboard	Supplementary Keyboard
NULL	NUL	0	CMND SH P	-
START OF HEADING	SOH	1	CMND A	-
START OF TEXT	STX	2	CMND B	-
END OF TRANSMISSION	ETX	3	CMND C	-
END OF TEXT	EOT	4	CMND D	-
ENQUIRY	ENQ	5	CMND E	-
ACKNOWLEDGE	ACK	6	CMND F	-
RING BELL	BEL	7	CMND G	-
DATA LINK ESCAPE	DLE	20	CMND P	-
DEVICE CONTROL 1	DCH1	21	CMND Q	-
DEVICE CONTROL 2	DC2	22	CMND R	-
DEVICE CONTROL 3	DC3	23	CMND S	-
DEVICE CONTROL 4	DC4	24	CMND T	-
NEGATIVE ACKNOWLEDGE	NAK	25	CMND U	-
SYNCHRONOUS IDLE	SYN	26	CMND V	-
END OF TRANSMISSION BLOCK	ETB	27	CMND W	-
BREAK	BRK	Sends Nulls	BREAK	-
SUBSTITUTE	SUB	32	CMND Z	-

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APPENDIX C

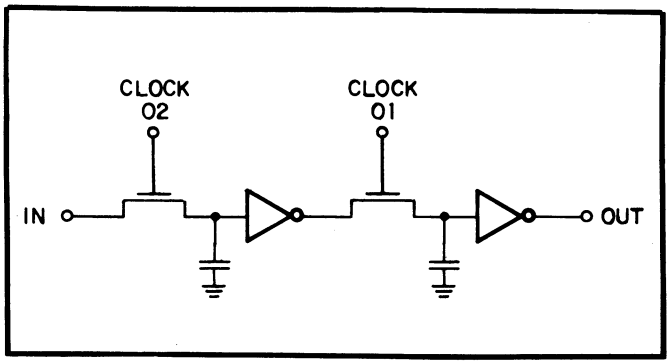
A REVIEW OF DYNAMIC SHIFT REGISTERS

INTRODUCTION

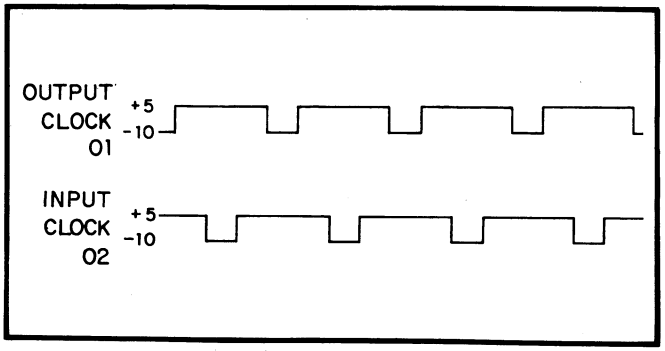
The DGC display uses 1024 bit MOS dynamic shift registers as main memory. These shift registers have certain design requirements, stemming from their design characteristics. These design requirements must be met in the display application.

DESIGN CHARACTERISTICS OF MOS DYNAMIC SHIFT REGISTERS

Dynamic MOS design of the display main memories requires that the shift registers be continuously recirculating to retain data. These registers are called two phase dynamic shift registers. This type of MOS shift register uses two stages to store each bit. A one bit storage element is called a shift register cell. Each stage of a shift register cell is basically an inverter with a capacitance to hold the data. Two non-overlapping clocks control the shifting of data. The first clock (clock 01) is used to load the first stage of the shift register as shown in the block diagram below.



When the first stage clock has finished clocking the data in, the second stage clock (clock 02) refreshes the second stage or output of the cell. The storage of data depends upon the continuous clocking of the alternate phases. If the clocks are stopped for too long a period, the capacitance will discharge and the cell can lose its information. The diagram below shows the necessary clock pulse characteristics. The display control logic operates the shift registers within design specifications.



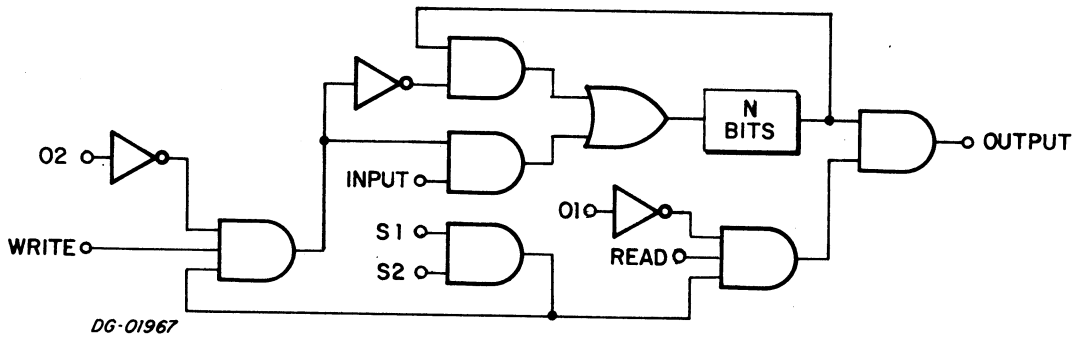
THE 1024 BIT RECIRCULATING SHIFT REGISTER

The 1024 bit register is made up of 1024 of these shift register cells plus logic to operate them. A block diagram of the system is shown below along with a truth table for the various control inputs.

REFERENCES

1. G. Lueke, J. P. Mitze, W. N. Carr; Semiconductor Memory Design and Application, Texas Instruments Electronics Series; McGraw-Hill Book Company, New York; c. 1973.

2. Signetics Catalog; 1973.



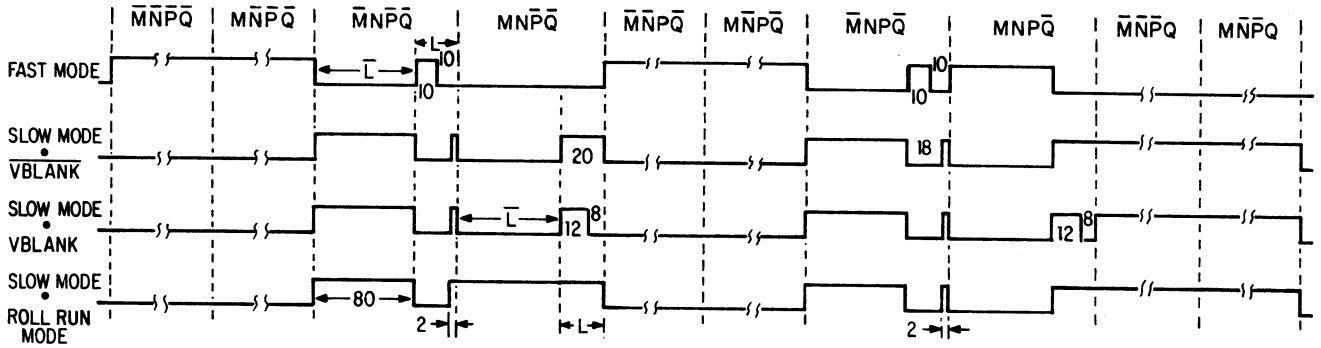
Truth Table

Write	Read	Function
0	0	Recirculate, Output is "0"
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is "0"
1	1	Read Mode, Output is Data

APPENDIX D

TIMING DIAGRAMS

MAIN MEMORY CLOCK GENERATION TIMING DIAGRAM



EACH SCAN COUNT (MNPQ)
EQUAL TO 100 CHAR CLOCKS

5/7 SLOW MODE ⟶ FAST MODE

$\overline{VBLANK}$

500 FAST ⟶	700	MAIN MEMORY CLOCKS
404 SLOW ⟶	404	" " "
96 STOP	1104	" " "
1000		

VBLANK

500 FAST ⟶	700	" " "
388 SLOW ⟶	388	" " "
112 STOP	1088	" " "
1000		

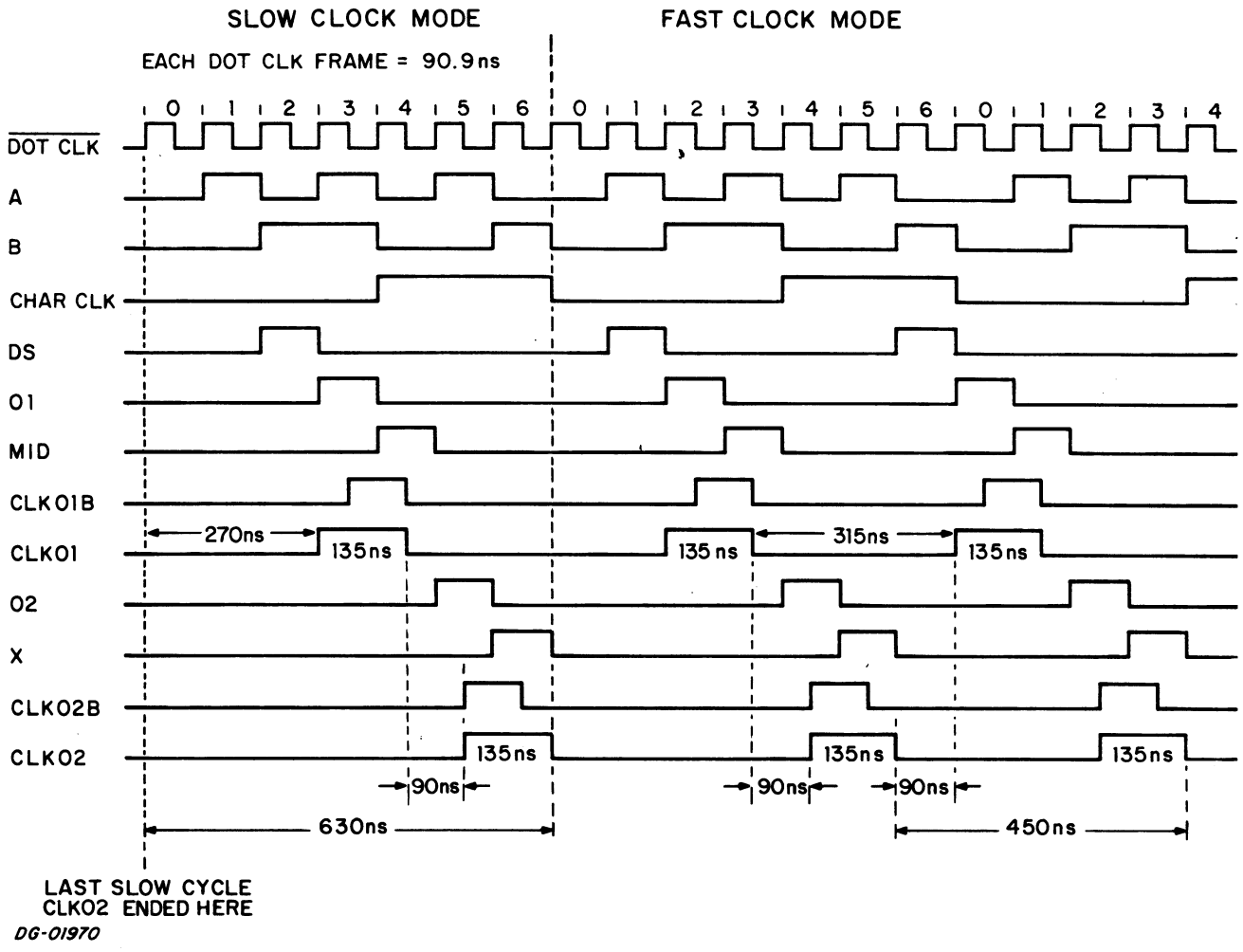
ROLL RUN MODE

500 FAST ⟶	700	" " "
484 SLOW ⟶	484	" " "
16 STOP	1184	" " "
1000		

CHAR CLOCK TALLY ⟵

DG-01971

÷7 DOT CLOCK CONVERSION TO DUAL MODE CLOCKS TIMING DIAGRAM



APPENDIX E
MAINTENANCE

INTRODUCTION

The DGC display requires very little maintenance. Some useful hints follow.

CLEANING

If it is necessary to clean the display, soap and water may be used to wash the exterior. Do not drop water on or near the keyboard as it may seep in and damage the contacts.

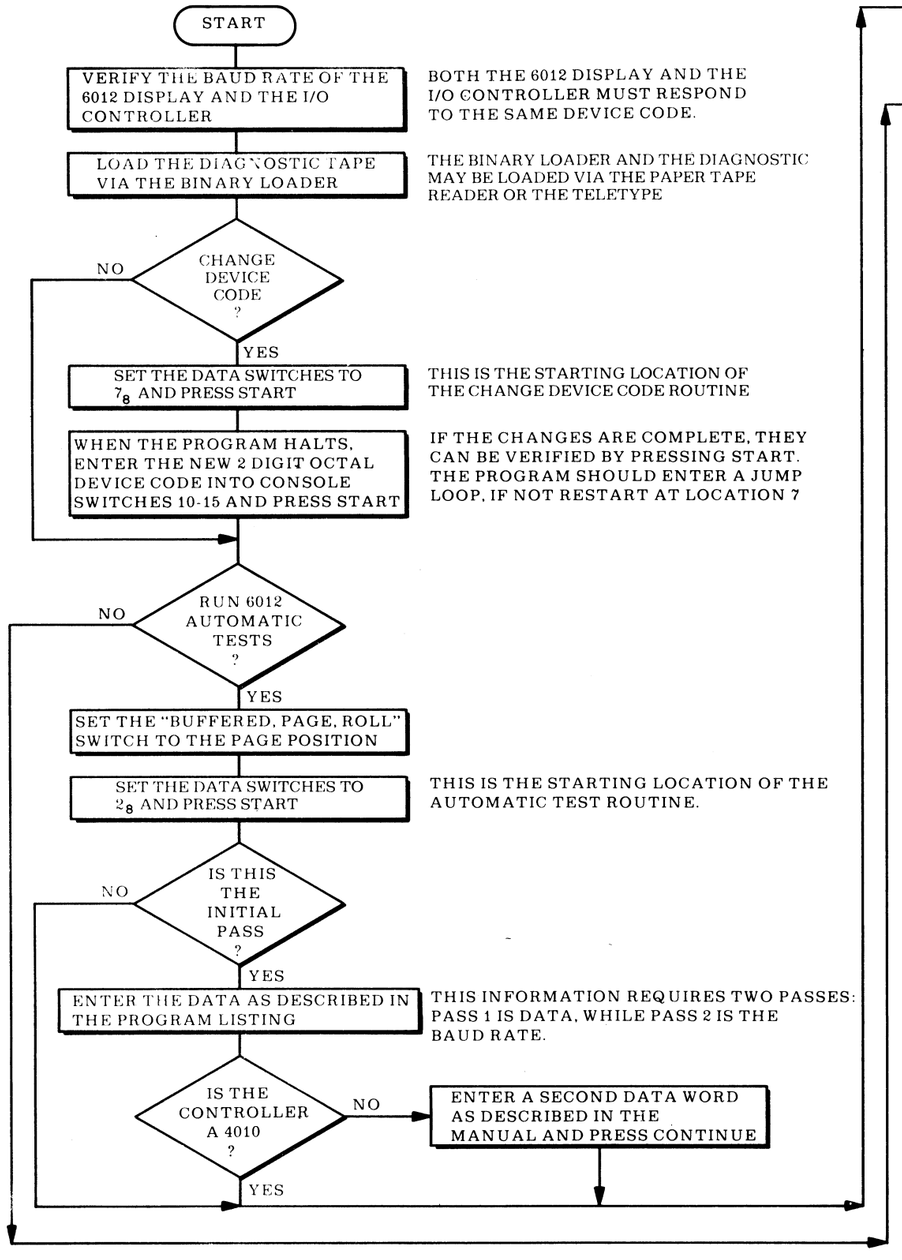
Caution The screen is made of plastic; it is possible to damage it by using incorrect cleaning solvents. Do not use alcohol or acetone based cleaners.

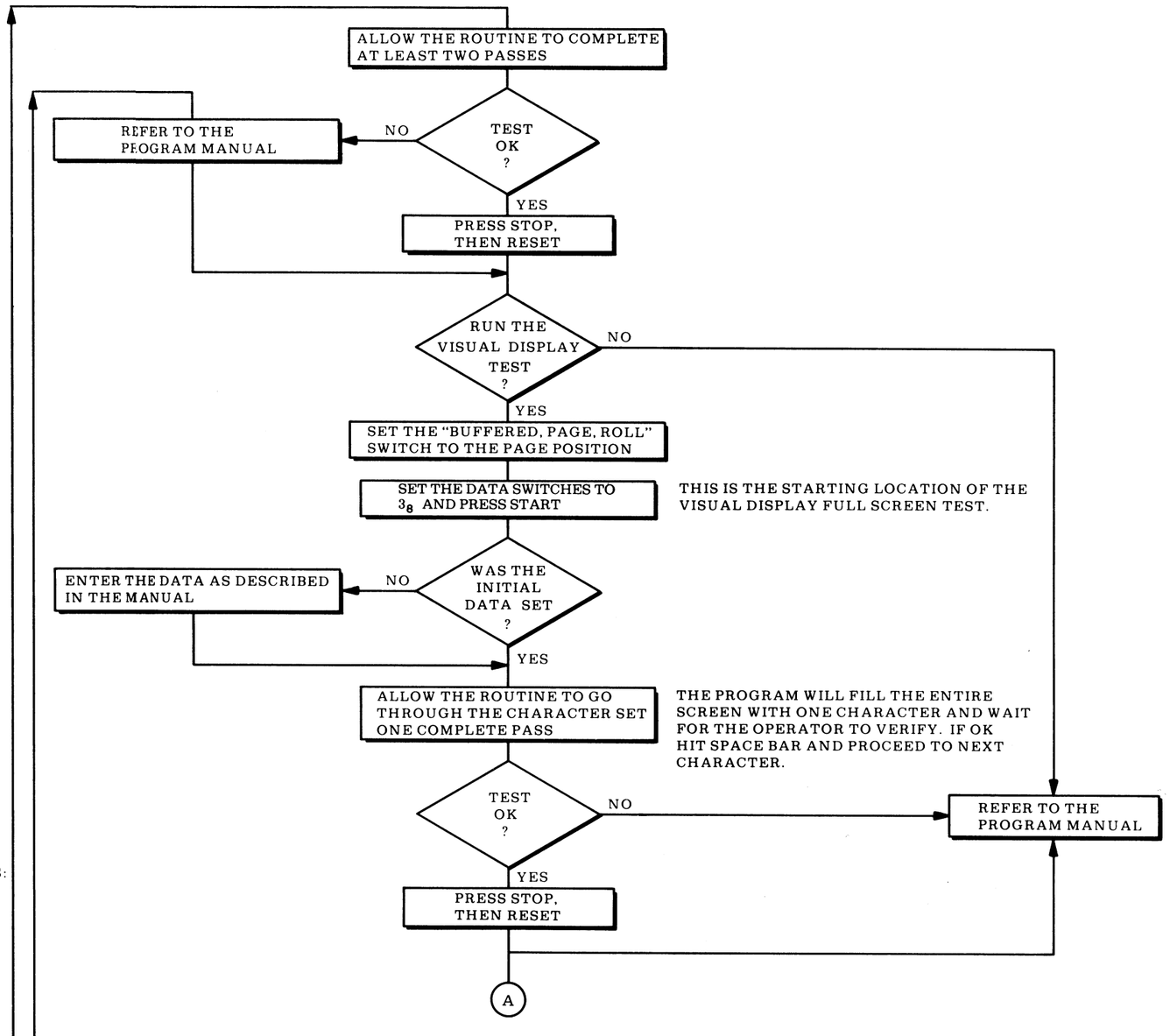
WORDS OF CAUTION

1. It is poor practice to use the equipment as a counter top, particularly for liquids like coffee and soft drinks.
2. Always check the line voltage before plugging an expensive piece of equipment into an unknown socket.
3. Always be aware that too much heat, moisture, or contaminents can harm the equipment.
4. Be very careful how cables are routed; they should never be strained, cramped or crushed (underfoot).
5. Be careful when working near or handling the cathode ray tube in the monitor; cracking it can cause an implosion of it.
6. There is a high voltage power supply in the video monitor. Do not try to handle or repair the monitor unless you have the necessary experience and knowledge.

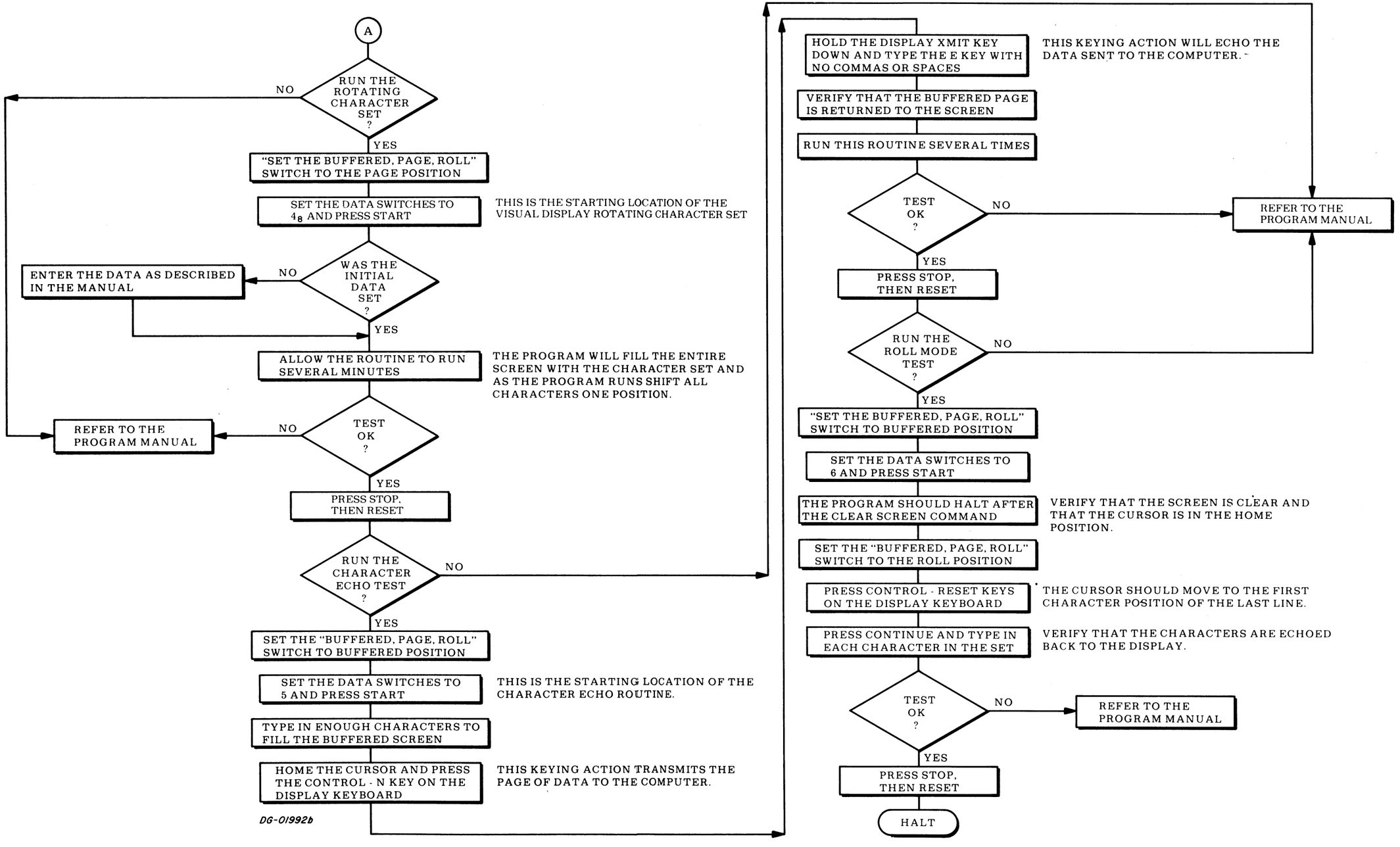
TESTING THE DGC DISPLAY

Data General supplies a diagnostic package to test the reliability of the display. This diagnostic package includes documentation procedures and binary programs for all of the diagnostic tests. The programs are used to test the logic and reliability of the display, while the manuals provide the necessary information for operating procedures, error interpretation, console switching settings, and areas tested. Following are the flowcharts of the procedure used to test the display.





DG-01992a



TROUBLESHOOTING

It is often convenient to have the display control board removed from the main chassis when troubleshooting the display. The following procedure should be followed when removing the control board from the main chassis.

1. Turn off the display and unplug the power cord.
2. Remove the cover of the display by unlatching the four latches on the underside of the main chassis, and carefully lifting the cover vertically off the chassis.
3. Unplug the edge connectors from the rear and side of the display control board, unplug the connector on the topside of the control board.
4. Remove the four screws at the corners of the display control board, and gently slide the board out of the main chassis.
5. Reconnect the edge connectors, and power plug to the display control board. The control board should be placed on a flat, nonconducting surface.
6. Plug the display in, and pull up the safety interlock switch located on the top of the display power supply. This allows the display to operate with the cover off.
7. Place the display in Local mode. With the display control board out of the main chassis, signals may be traced more easily.

Caution Remember, the monitor power supply operates at 12,000 volts. Keep away from the monitor when operating the display without its cover.

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